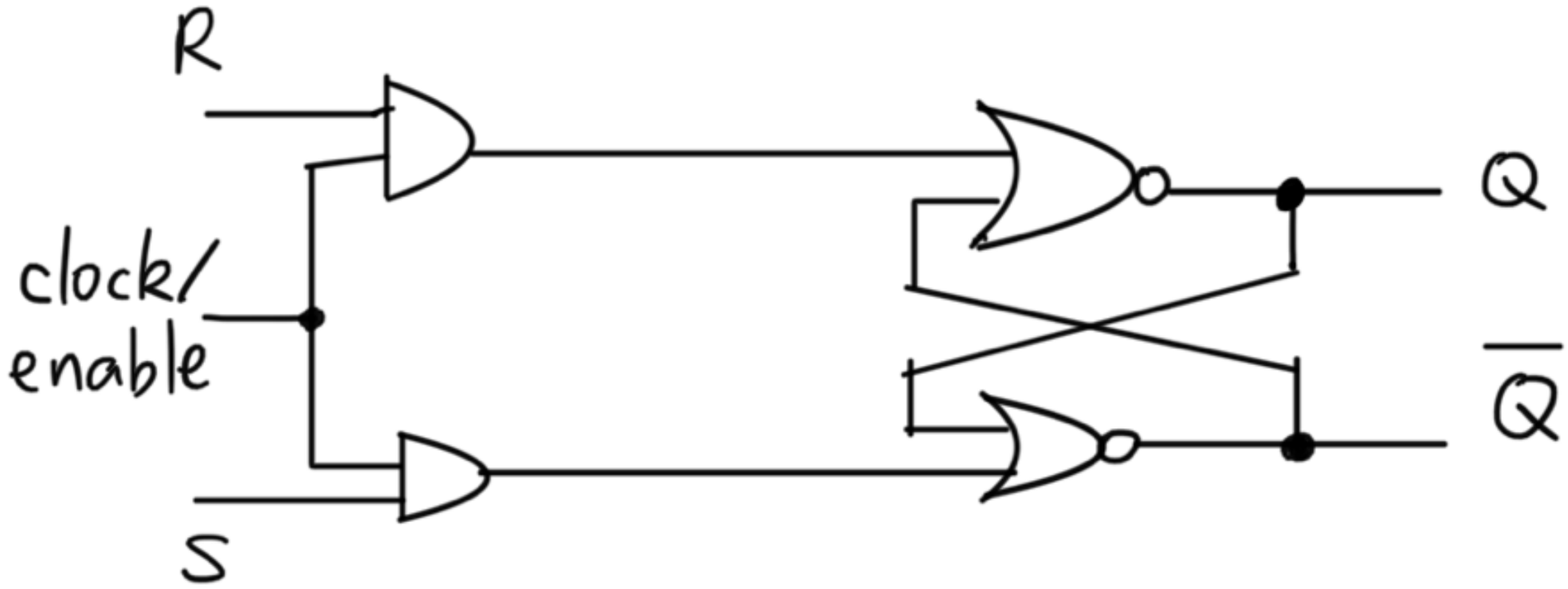
Digital Logic and Computer Organization

Sequential Logic — Gated Latches

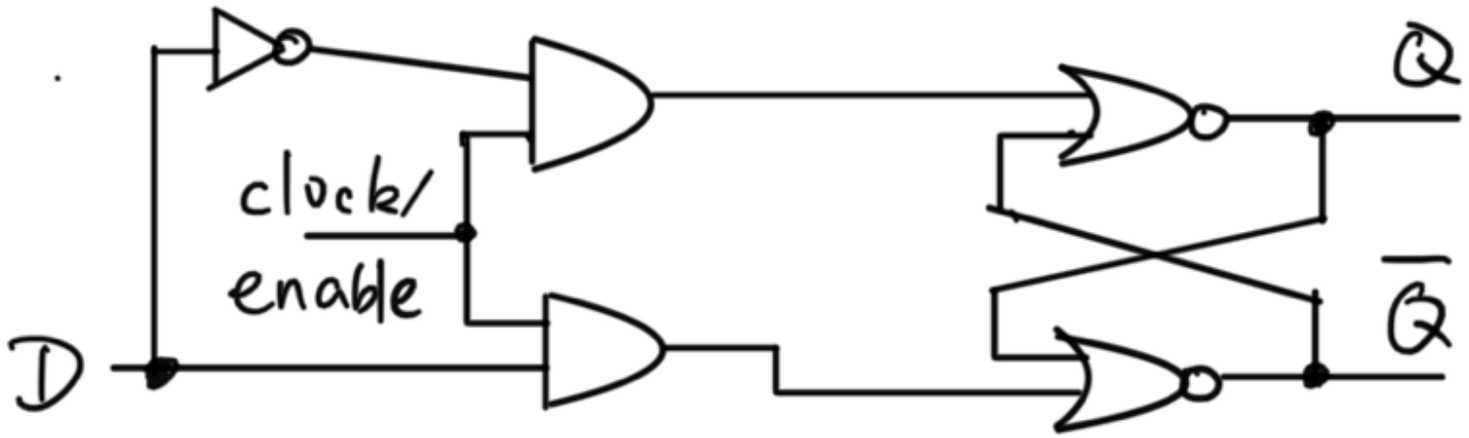
Asynchronous Problems

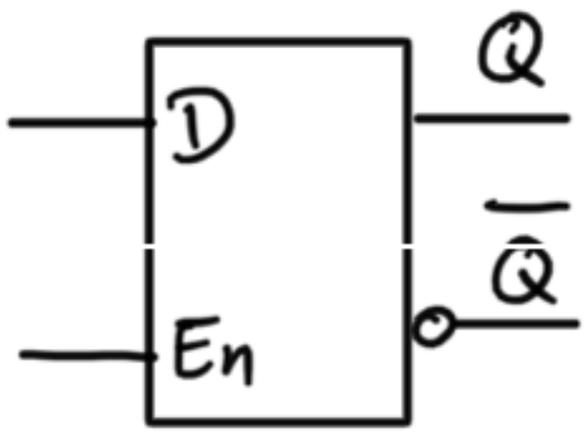
- Latches are asynchronous memory elements;
- Latch outputs are updated whenever its inputs change according to the appropriate characteristic equation;
- Problem: erratic state changes (think about the JK latch when JK = 11, or T latch when T = 1);
- How to fix it?
  - impose a synchronous timing discipline
  - add an enable (clock) signal as a gate keeper

Gated SR Latch

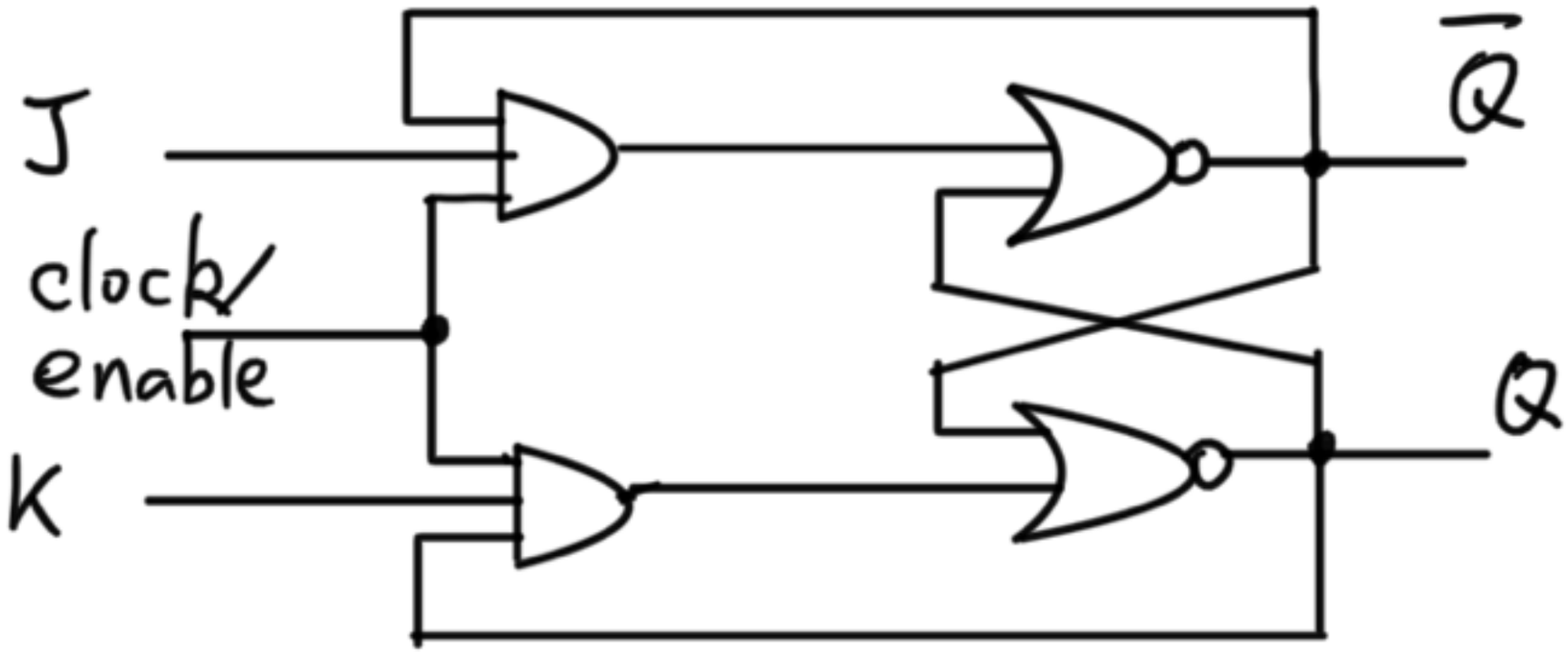


Gated D Latch





Gated JK Latch



Gated T Latch