Digital Logic and Computer Organization

Lab Introduction

Design Process

- specification
- truth table/
- boolean expression
- simplification
- schematic diagram
- simulation or implementation
- testing, debugging
- report

Verilog

- C like language
- module — class : describes a hardware component
- input and output ports
- variables — wires, regs
- structural and behavioural

Verilog on CSCI

- Compiling verilog code
  iverilog -o output.vvp topmodule.v

- Running the simulation
  vvp output.vvp

- Viewing the waveform and verifying verilog desing
  gtkwave dumpedwavefile.vcd

Hardware

- Lab Evaluator
- Breadboard
- Chips

Lab Report Standard

- Requirement(s)
- Behavioural Description
- Design
- If verilog simulation is required
    - structural or behavioural simulation
    - test bench simulation
    - test result waveform
- If implementation is required
    - Preparation
    - Breadboard pin-out
    - Implementation on breadboard
    - Test result observation