Computer Science CSCI 261

Computer Architecture and Assembly Language

Dr. Peter Walsh
Department of Computer Science
Vancouver Island University
peter.walsh@viu.ca

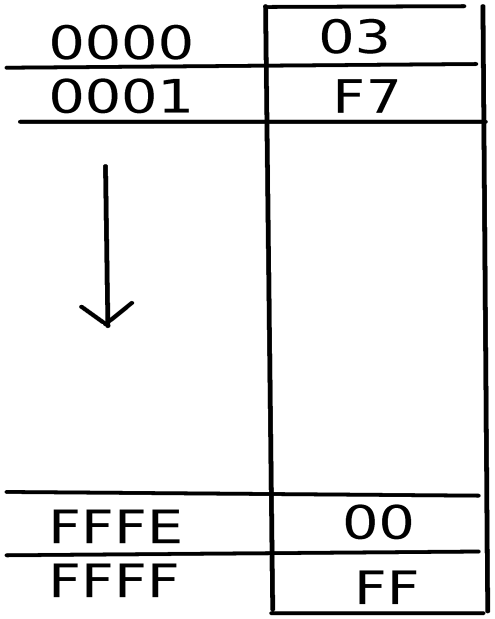
Computer Architecture

- Instruction Set Architecture (ISA)
  - abstract model of a computer
  - programmer's view of a computer
  - protocol that defines how a computer appears to a machine/assemble language programmer or a compiler
- ISA Components
  - memory model
  - instruction types
  - instruction codes

Memory Model

- Memory and Register Layout

e.g. 16 bit address space -- 8 bit data



PC (16 bits)

0001

03

R0 (8 bits)

8 bit machine

Instruction Types

- Data Movement
  - e.g. `load` and `store`
- Data Transformation
  - e.g. `add` and `sub`
- Conditional
  - e.g. `jnz` (conditional jump instruction)
- Input/Output
  - e.g. `ain` (read an ascii character for a serial device)

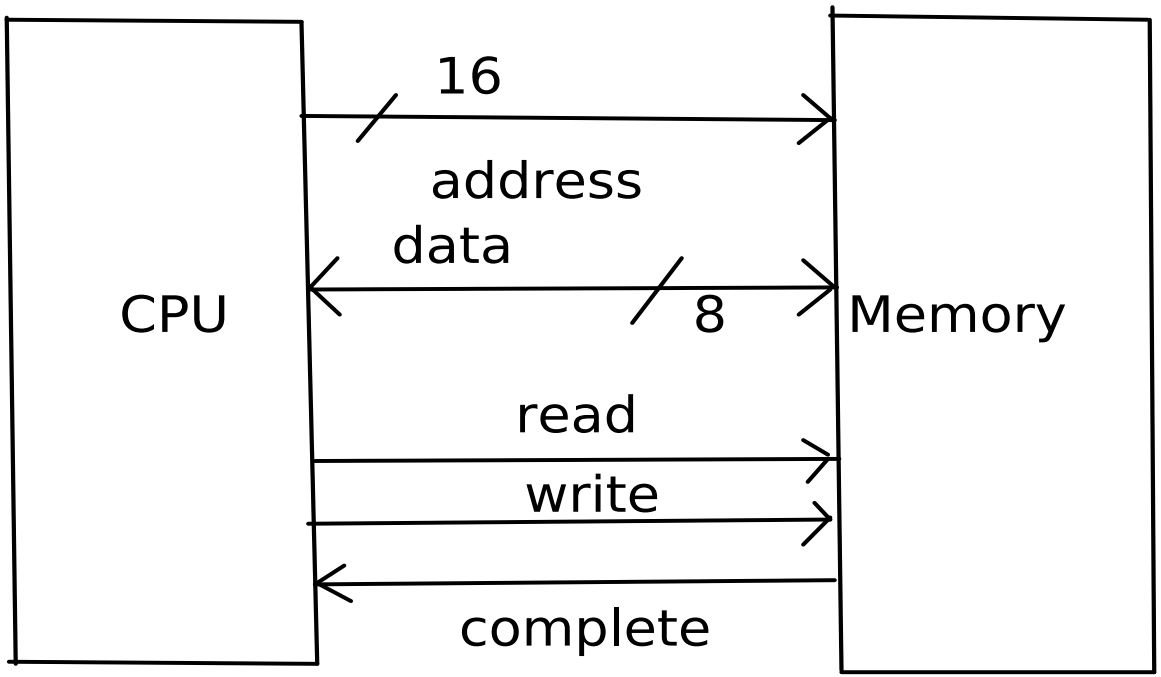
Instruction Codes

The following must be encoded in an instruction either explicitly or implicitly:

- which operation to perform
- where to find the operands
- where to put the results
- where to find the next instruction

Memory Read/Write Cycle

- e.g 16 bit address space — 8 bit data

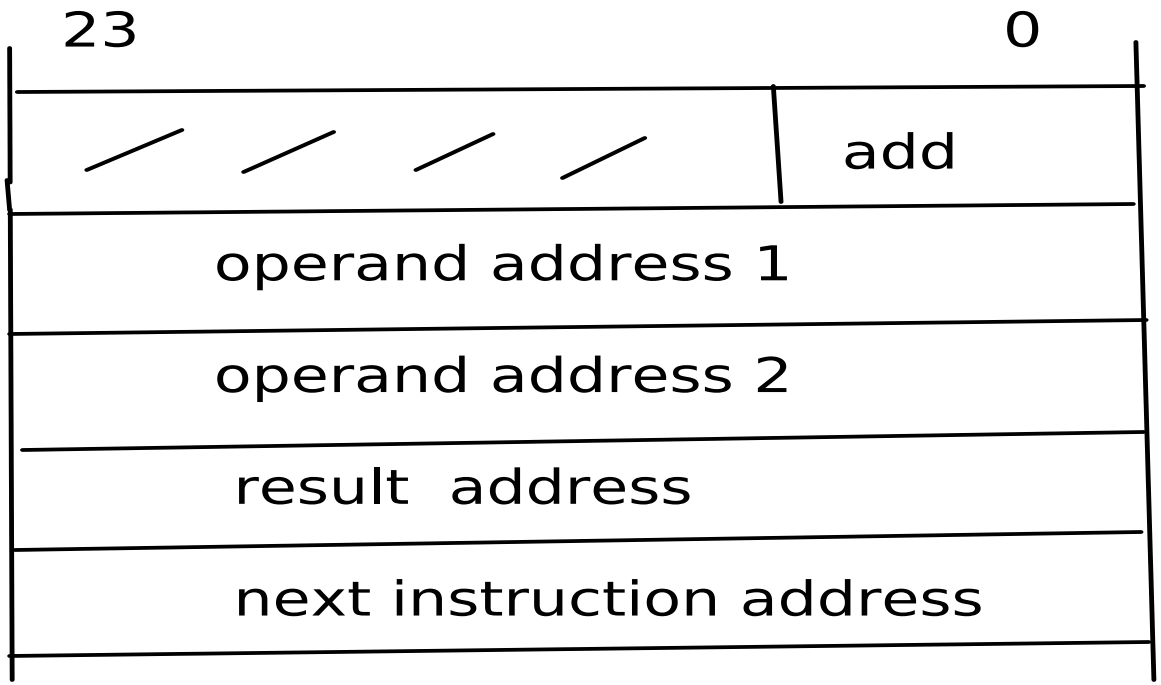


Machine Classification

Consider a hypothetical machine and its `add` instruction:

- 24 bit address space (3 bytes)
- 24 bit data (3 bytes)
- 128 instructions (7 bits rounded to 8)
- no programmer accessible registers

4-Address Machine

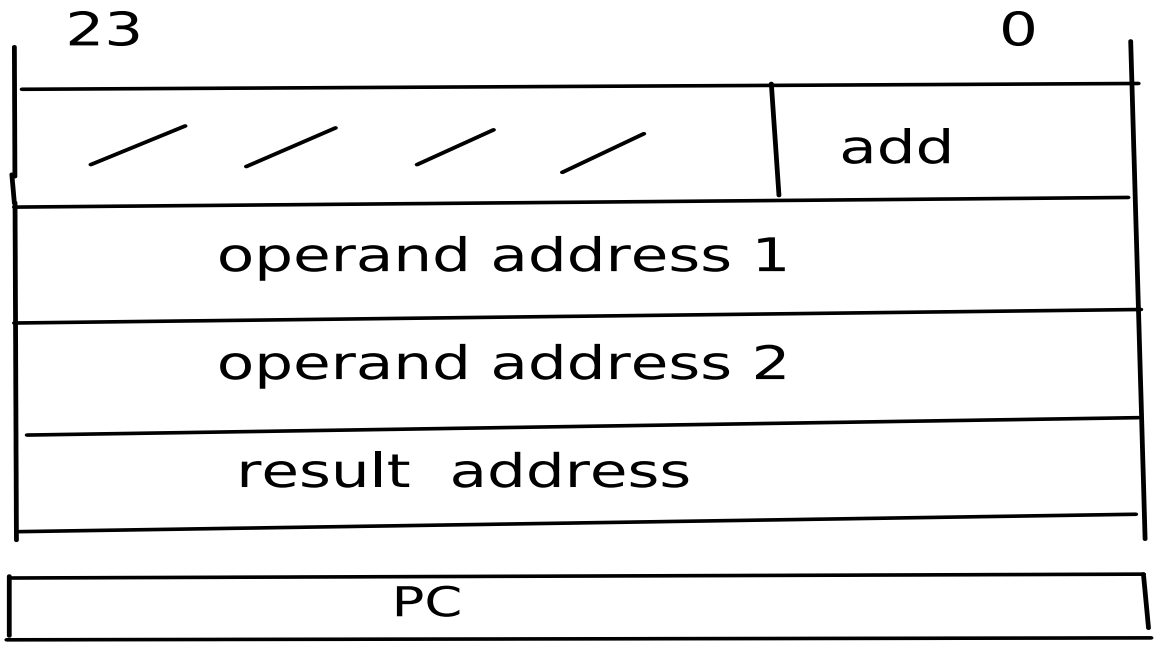


4-Address Machine cont.

- Instruction Fetch
  - 5 memory read cycles
- Operand Fetch
  - 2 memory read cycles
- Result Write
  - 1 memory write cycle
- Total
  - 8 read/write cycles

3-Address Machine

Include a register called a Program Counter (PC) that always points to the next instruction to be executed (except for branch instructions).

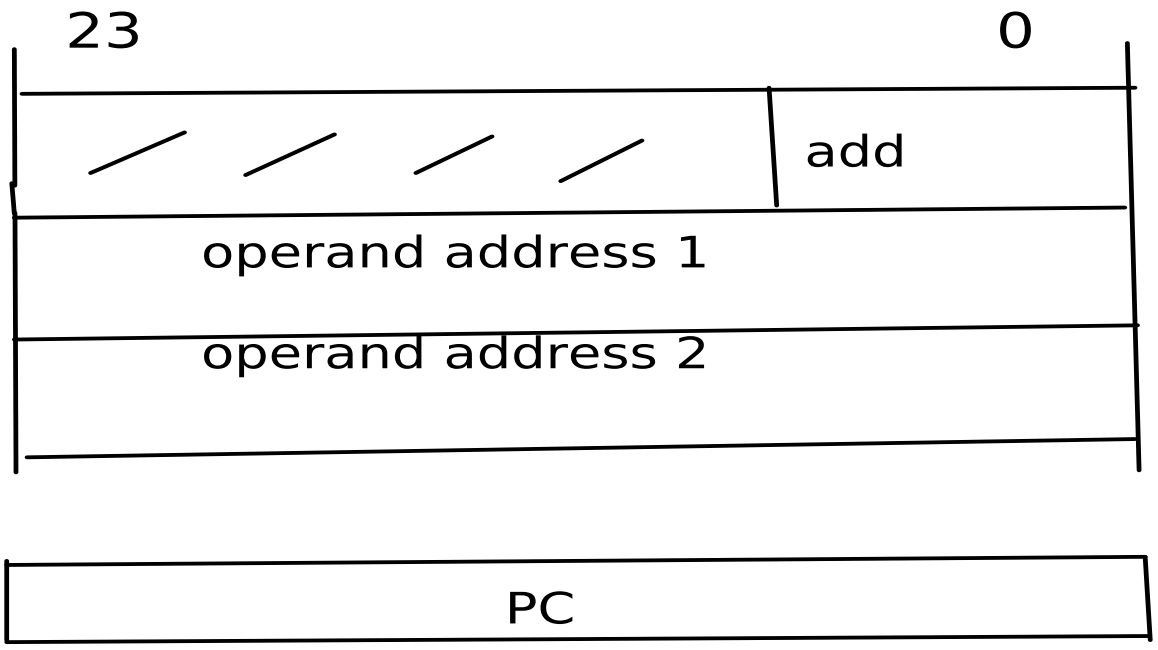


3-Address Machine cont.

- Instruction Fetch
  - 4 memory read cycles
- Operand Fetch
  - 2 memory read cycles
- Result Write
  - 1 memory write cycle
- Total
  - 7 read/write memory cycles

2-Address Machine

Store the result at the address of one of the operands.

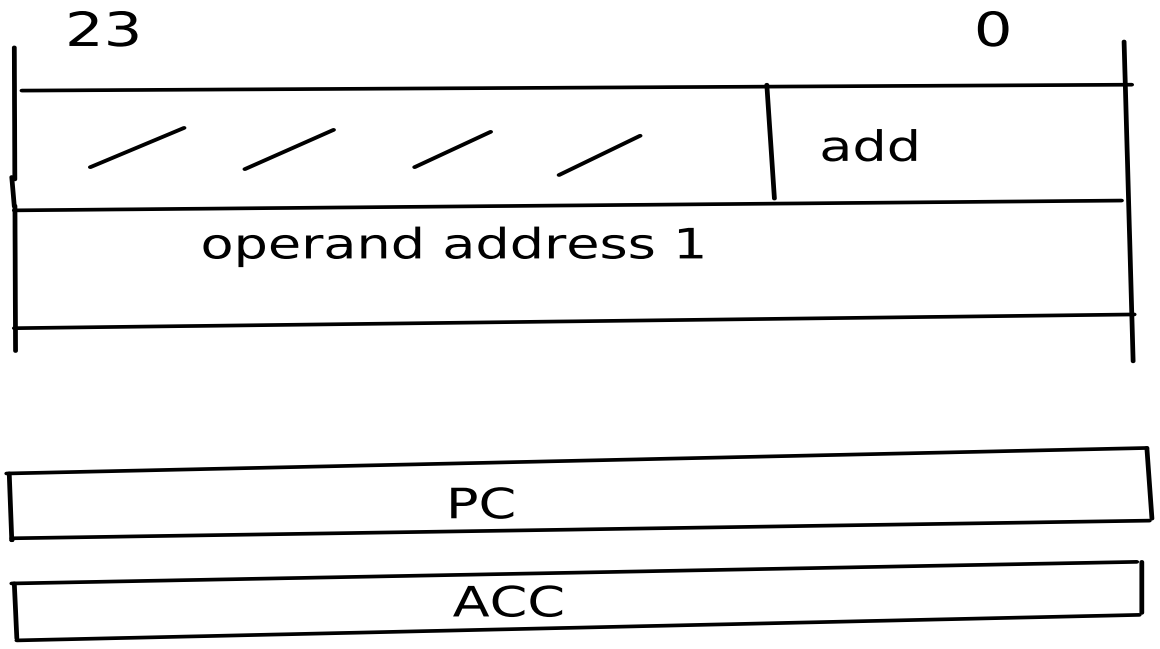


2-Address Machine cont.

- Instruction Fetch
  - 3 memory read cycles
- Operand Fetch
  - 2 memory read cycles
- Result Write
  - 1 memory write cycle
- Total
  - 6 memory read/write cycles

1-Address Machine

Include a register called an Accumulator (ACC) which becomes an instruction's implicit source and destination of data.

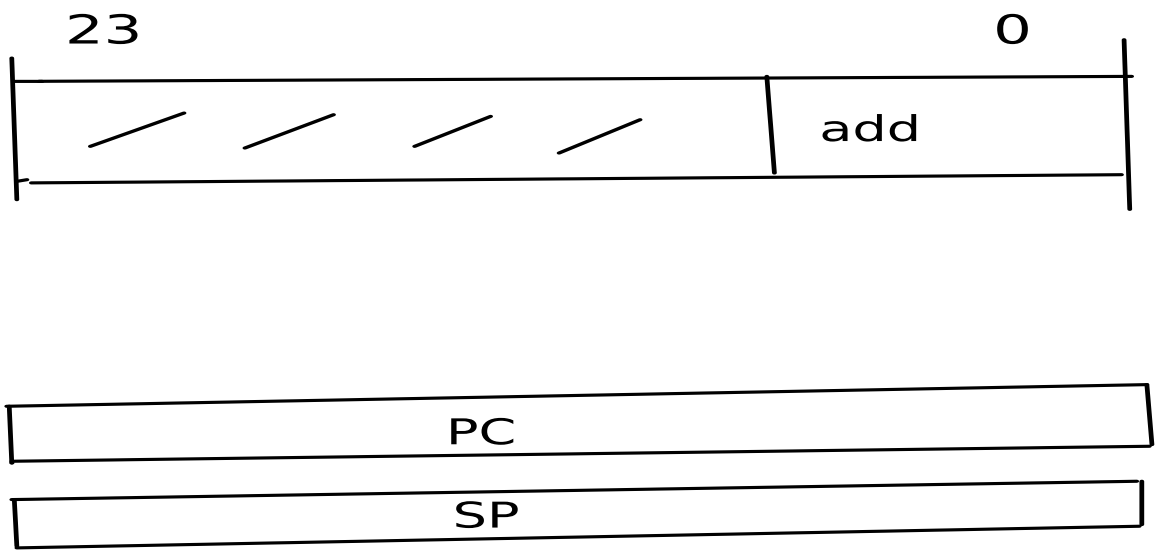


1-Address Machine cont.

- Instruction Fetch
  - 2 memory read cycles
- Operand Fetch
  - 1 memory read memory cycle
- Total
  - 3 memory read/write cycles

0-Address Machine

Include a register called a Stack Pointer (SP) which points the first free position in memory (top) of a push-down stack. The stack becomes an instruction's implicit source and destination of data.

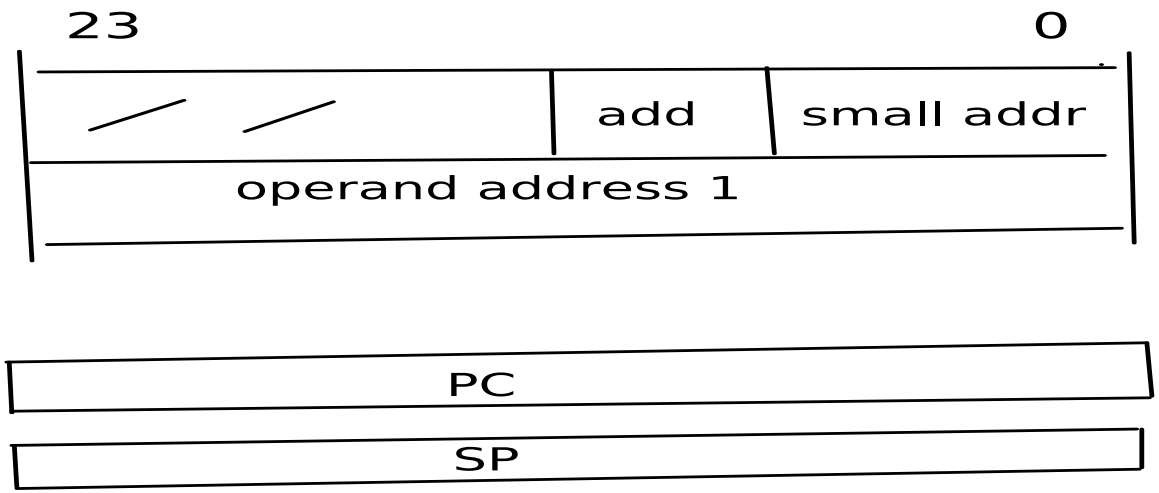


0-Address Machine cont.

- Instruction Fetch
  - 1 memory read cycles
- Operand Fetch
  - 2 memory read cycle
- Result Write
  - 1 memory write cycle
- Total
  - 4 memory read/write cycles

1.5-Address Machine

Include n general registers addressed by $log_2 n$ bit address (known as a small or half address). For example, 32 general registers would require a 5 bit half address.



1.5-Address Machine cont.

- Instruction Fetch
  - 2 memory read cycles
- Operand Fetch
  - 1 memory read cycle
- Total
  - 3 memory read/write cycles

Architecture Comparison

- Trade-Offs
  - code size
  - code functionality
  - time to execute (memory read/write cycles)

All machines exhibit some features if all the machine types. Since 1980, machines tent to have a general register organization.