Experiment 2

With reference to the Verilog description in `Lab2/ttl.v`:

Task (T1): Extract the IC logic schematic from the Verilog description.

Deliverable (D1): IC logic schematic.

Task (T2): Extract the combinational logic schematic.

Deliverable (D2): Logic schematic.

Task (T3): Perform symbolic analysis.

Deliverable (D3): Network expression specifying the output in terms of its inputs.

Task (T4): Perform literal analysis.

Deliverable (D4): Truth table with one output column for each of `I1, I2, I3, I4` and `E`.

Task (T5): Derive a minimal SOP expression for the modeled circuit.

Deliverable (D5): A listing of all the prime-implicants, the essential prime-implicants and the secondary prime-implicants. A minimal SOP expression and a K-Map showing the corresponding implicant cover.

Task (T6): Develop a testbench for the modeled circuit You must use a gold function as exemplified in the testing of SN7400. You must use your minimal SOP expression as the gold function.

Deliverable (D6): Electronic submission of source code (`make submit`).

Task (T7): Specify IC interconnections.

Deliverable (D7): One completed pin-out sheet (at least) for each IC employed in the physical design.

Task (T8): In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D8): A physical realization of the combinational system that behaves to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task (T9): Document any relevant results, explanations or comments.

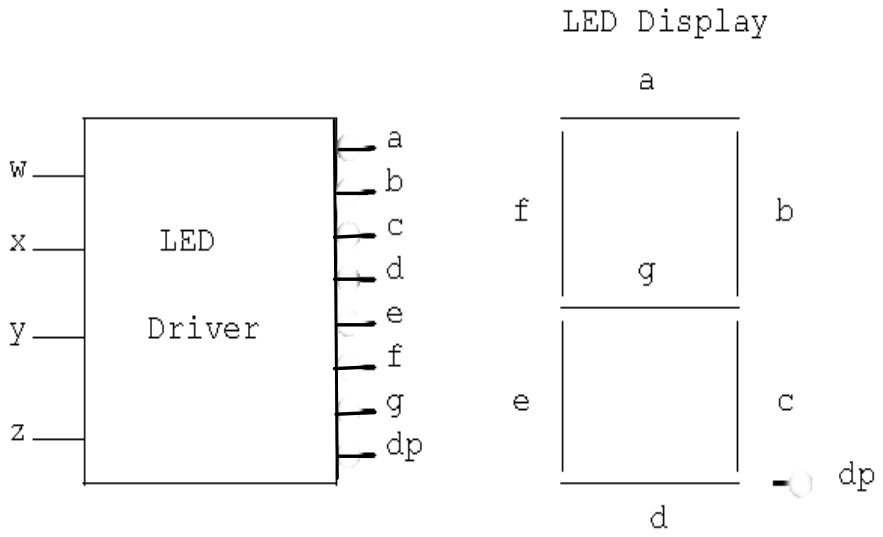
Deliverable (D9): A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

NOTES

Experiment 3

A seven segment display is used to display a decimal digit (or a hex digit). Such displays are often found in electronic watches, clocks and appliances. The seven segment display used in this lab consists of seven LED segments and a decimal point (see Breadboard manual).

Consider the combinational system (LED Driver) and the seven segment display (LED Display) depicted in the following logic schematic:



The LED Driver takes as input, a four bit binary number (`w,x,y,z` with `z` the LSB) and produces active high output to drive the LED Display. If the input is between `0000` and `1001` inclusive then the LED Display's decimal point `dp` is illuminated.[1] If the input is between `1010` and `1111` inclusive then the LED Display's decimal point `dp` is not illuminated and the LED Display's segments `a` through `g` are illuminated so as to display the hex character (in upper case) that represents the input. For example, if the input is `1111` then the segments `a`, `e`, `f` and `g` are illuminated. All other segments (including the decimal point `dp`) are not illuminated.

Task (T1): Perform problem analysis.

[1] illuminated means the associated input signal is asserted (active high)

Deliverable (D1): Truth table for the LED Driver with one output column for each of `a, b, c, d, e, f, g` and `dp`.

Task (T2): Use espresso to derive a minimized SOP expression for the LED Driver.

Deliverable (D2): Hardcopy of espresso input and output.

Task (T3): Perform symbolic analysis.

Deliverable (D3): Logic schematic derived from espresso output and a network expression specifying LED driver output in terms of its inputs.

Task (T4): Develop a structural Verilog model of the LED Driver using the Verilog models for the TTL ICs SN7432, SN7408 and SN7404.

Deliverable (D4): Electronic submission of source code (`make submit`).

Task (T5): Map your Verilog model to an IC-based physical design using TTL components and one of the seven segment displays on your breadboard.

Deliverable (D5): IC logic schematic.

Task (T6): Specify IC interconnections.

Deliverable (D6): One completed pin-out sheet (at least) for each IC employed in your physical design.

Task (T7): In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D7): A physical realization of the combinational system that behaves to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task (T8): Document any relevant results, explanations or comments.

Deliverable (D8): A section in your report entitled Results/Explanations/Comments in

which you have detailed any relevant results, explanations or comments.

NOTES

Experiment 4

Consider again the combinational system (LED Driver) and the seven segment display (LED Display) from Experiment 3. The LED Driver takes as input, a four bit binary number (`w,x,y,z` with `z` the LSB) and produces active high output to drive the LED Display. For this experiment, if the input is between `0000` and `1001` inclusive then the LED Display's segments `a` through `g` are illuminated so as to display the decimal character that represents the input.[2] The LED Display's decimal point `dp` is NOT illuminated. See the testbench to determine the exact segment pattern for each decimal digit.

Task (T1): Perform problem analysis.

Deliverable (D1): Truth table for the LED Driver with one output column for each of `a, b, c, d, e, f, g` and `dp`.

Task (T2): Design a ROM to implement the LED Driver. Use a decoder and glue logic to implement the ROM. The glue logic must be composed of either `and` gates, `or` gates, `nand` gates or `nor` gates.

Deliverable (D2): A logic schematic of your solution.

Task (T3): Develop a structural Verilog model of the LED Driver. You are required to use the Verilog model for the TTL IC SN74154 and any other TTL models of your choosing.

Deliverable (D3): Electronic submission of source code (`make submit`).

Task (T4): Map your Verilog model to an IC-based physical design using TTL components.

Deliverable (D4): IC logic schematic.

Task (T5): Specify IC interconnections.

Deliverable (D5): One completed pin-out sheet (at least) for each IC employed in your

[2] illuminated means the associated input signal is asserted (active high)

physical design.

Task (T6): In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D6): A physical realization of the combinational system that behaves to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task (T7): Document any relevant results, explanations or comments.

Deliverable (D7): A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

NOTES