

# Computer Science CSCI 355

## Digital Logic and Computer Organization

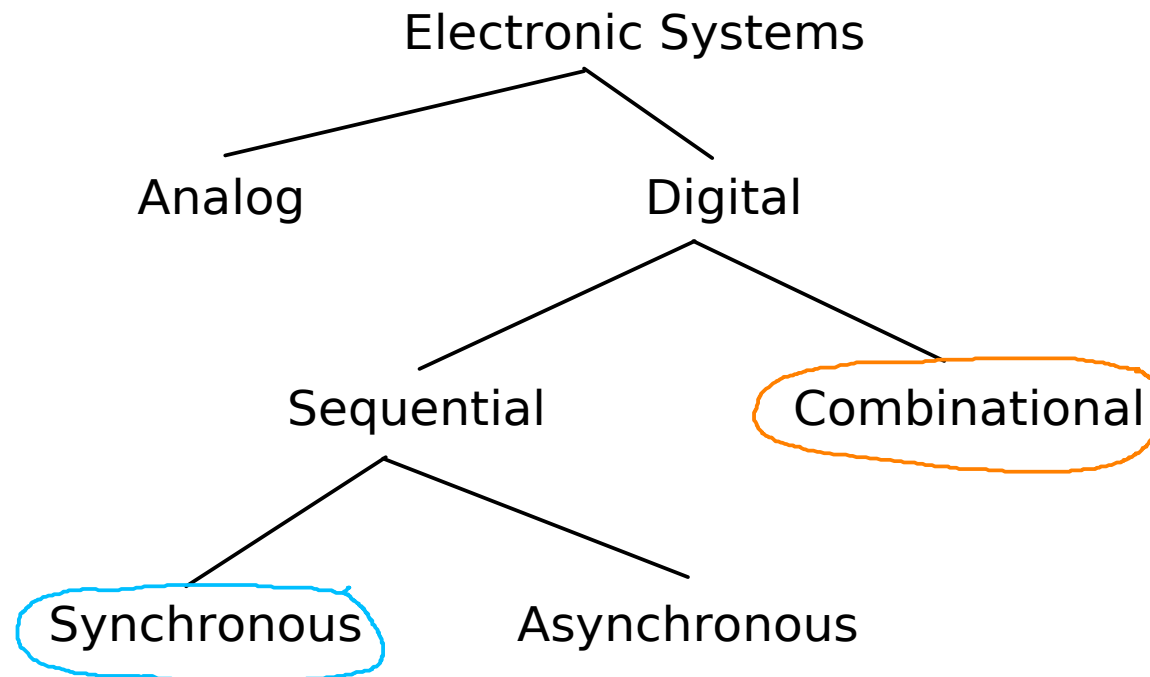
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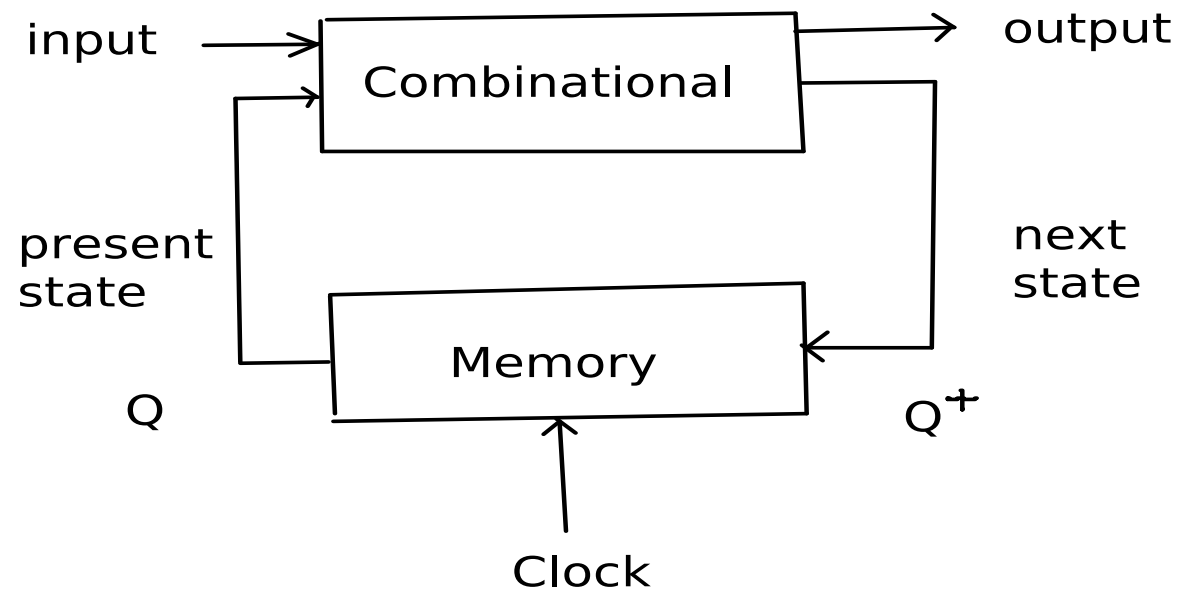
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# Sequential Systems



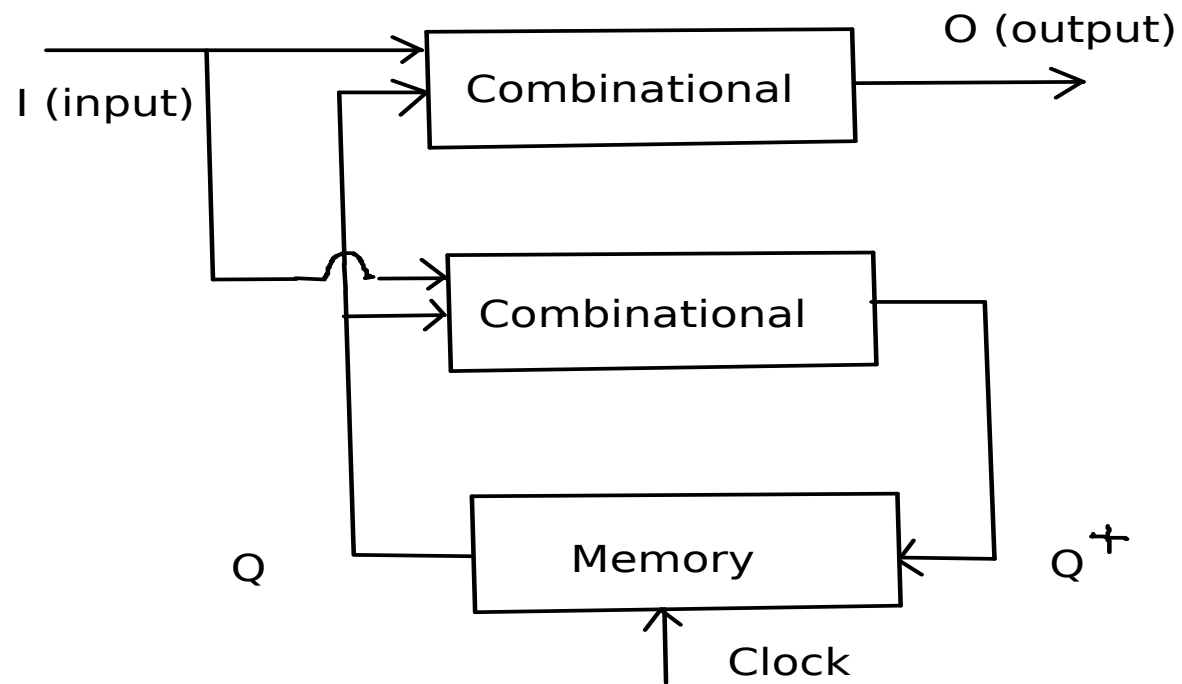
# Synchronous Sequential Systems

- Combinational System Plus Memory
  - synchronous (clocked)
  - asynchronous (self timed)



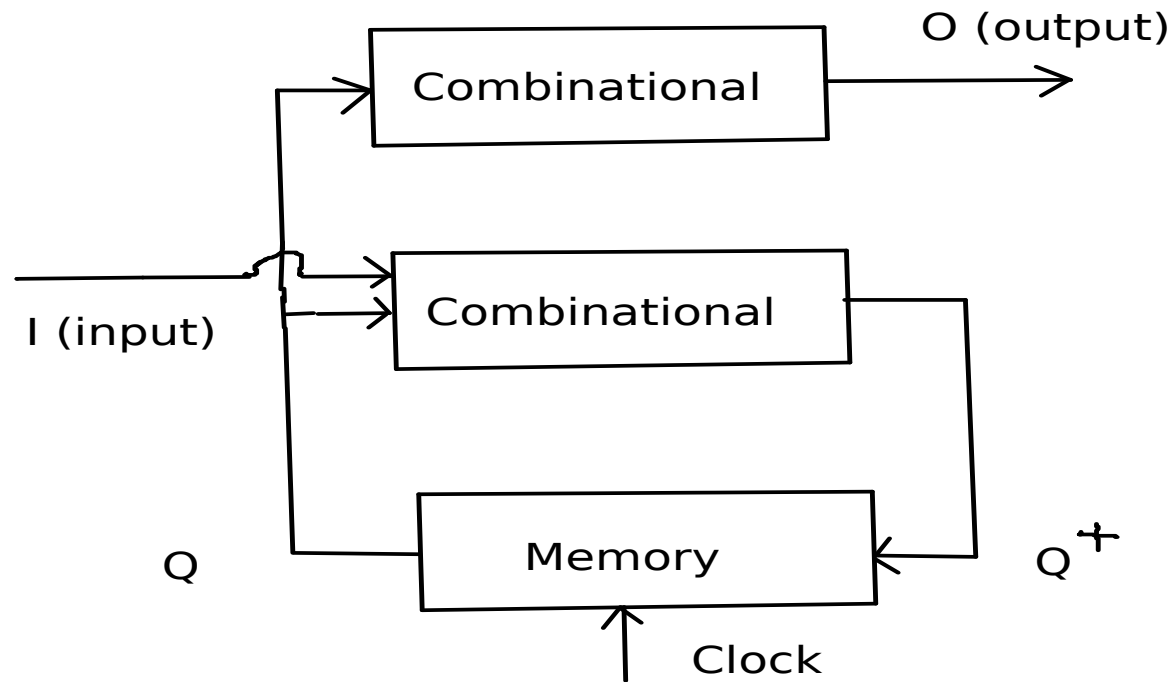
# Mealy Machine

- $O = f(I, Q)$
- $Q^+ = f(I, Q)$



# Moore Machine

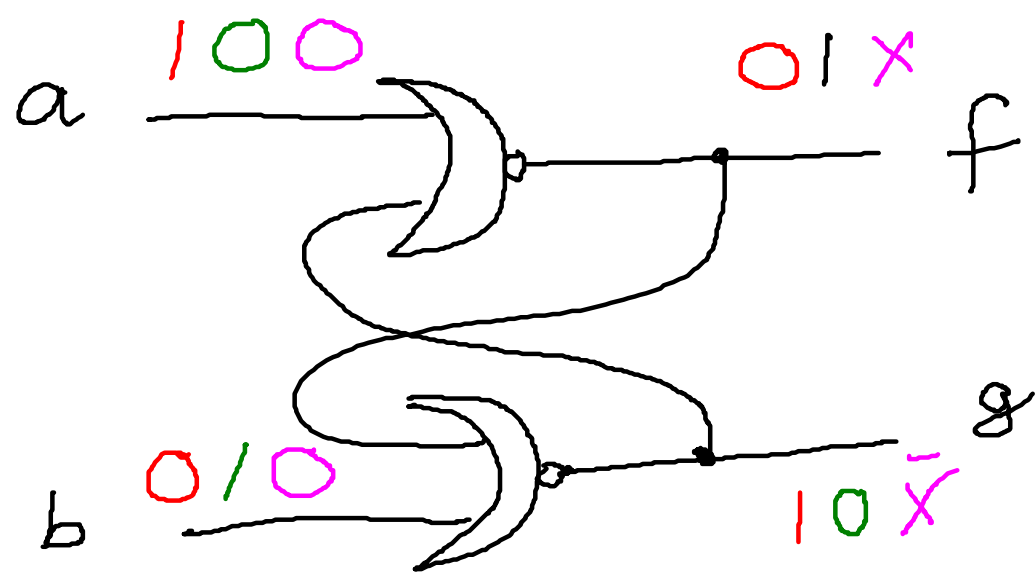
- $O = f(Q)$
- $Q^+ = f(I, Q)$



## Memory Devices

- Dynamic RAM (DRAM)
  - constructed using a transistor and a capacitor
  - needs continual cell recharging
  - capable of higher densities than SRAM
  - slower than SRAM
  - consumes more power than SRAM
- Static RAM (SRAM)
  - constructed using transistors
  - no need for continual cell recharging
  - capable of lower densities than DRAM
  - faster than DRAM
  - consumes less power than DRAM
  
  - latches (ungated and gated)
  - flip flops (pulse triggered and edge triggered)

# Cross Coupled Nor Gates



$x$	$y$	NOR
0	0	1
0	1	0
1	0	0
1	1	0

# SR Latch (Set, Reset)

S R Q Q<sup>+</sup>

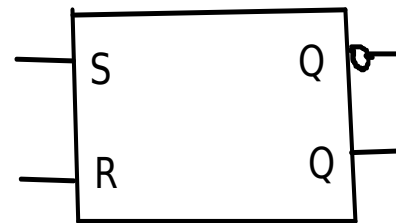
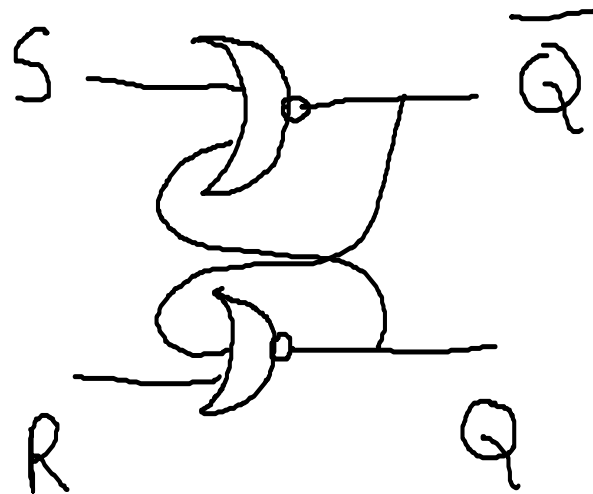
a	b	f	g	f <sup>+</sup>	g <sup>+</sup>
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	0	1

Handwritten truth table for SR Latch:

S	R	Q <sup>+</sup>
0	0	Q
0	1	0
1	0	1
1	1	1



# SR Latch cont.



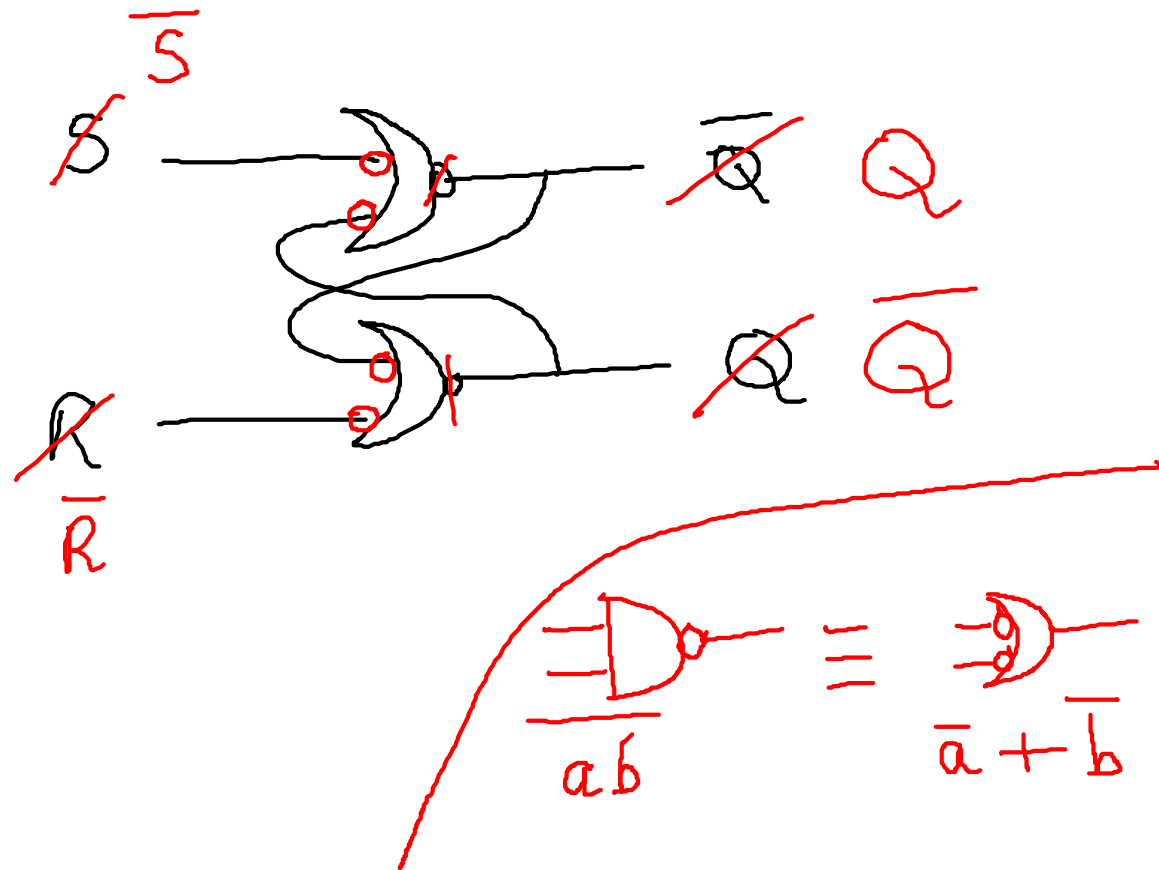
		R Q			
		00	01	11	10
S	0	0	1	0	0
	1	1	1	-	-

$Q^+$

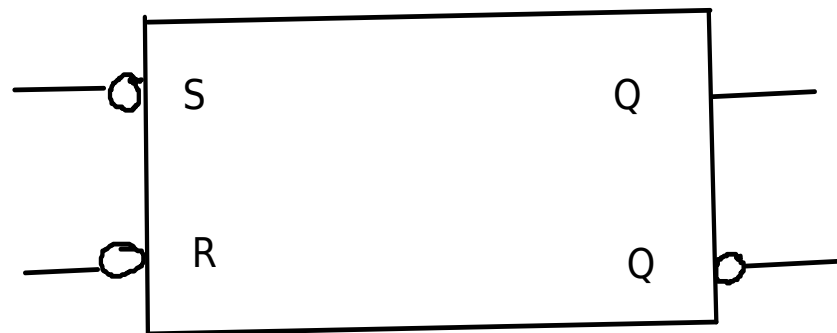
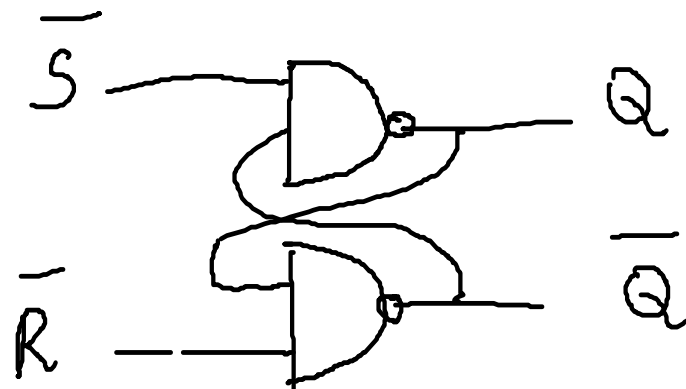
Characteristic Equation

$$Q^+ = S + R'Q$$

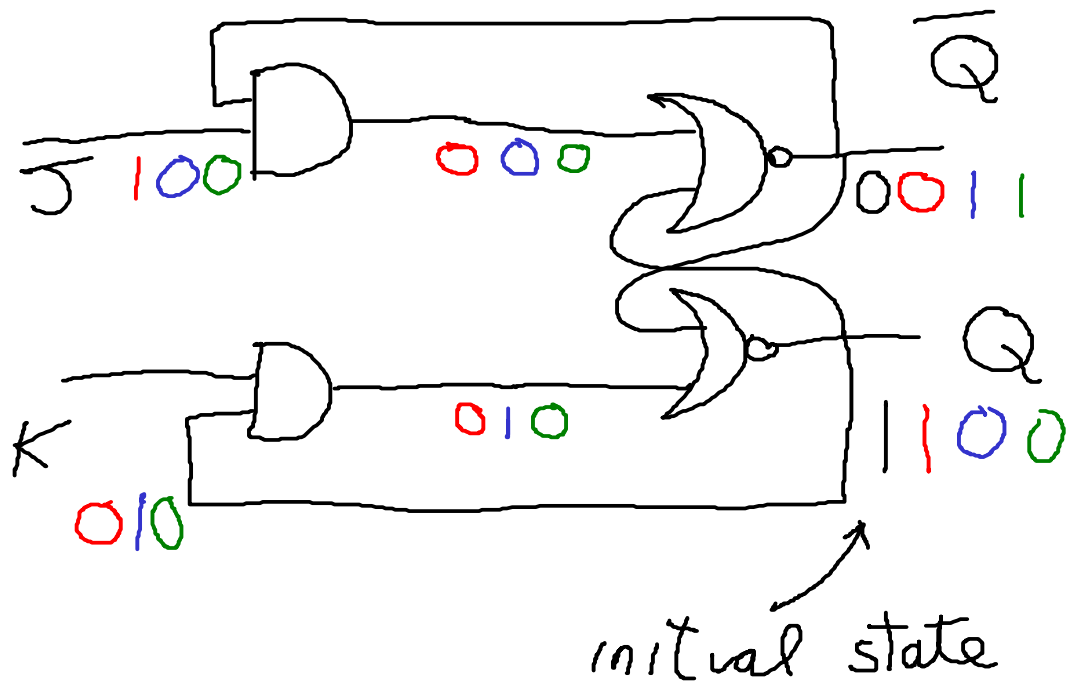
# SR Latch (Nand Implementation)



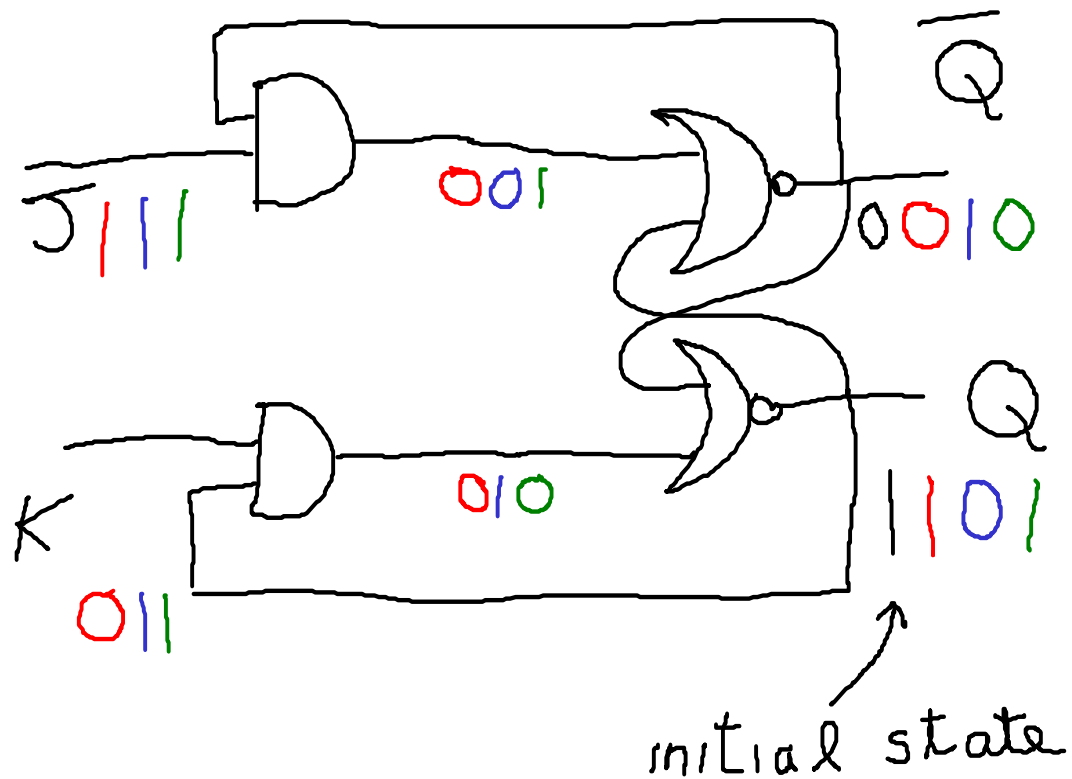
# SR Latch (Nand Implementation) cont.



# JK Latch (Jack Kilby)



# JK Latch cont.



## JK Latch cont.

J	K	$Q^+$
0	0	Q
0	1	0
1	0	1
1	1	$Q'$

		K Q			
		00	01	11	10
J	0	0	1	0	0
	1	1	1	0	1

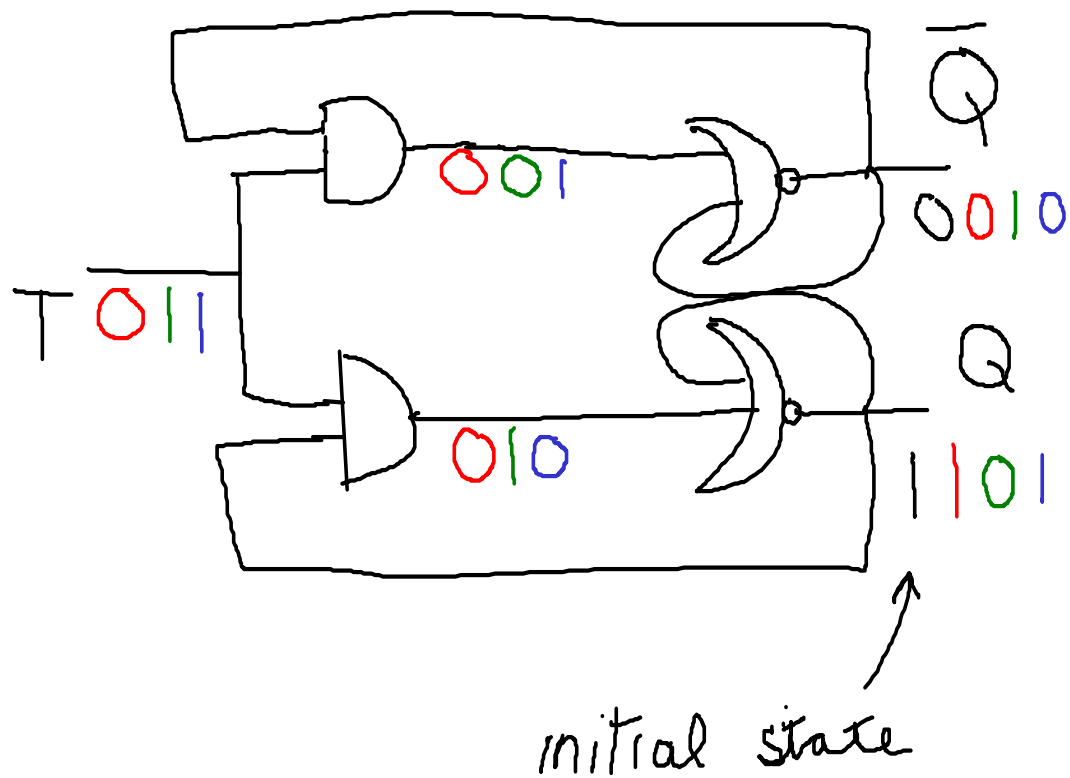
$Q^+$

Problem  
 $JK = 11$   
Output Oscillates

Characteristic  
Equation

$$Q^+ = JQ' + K'Q$$

# T Latch (Toggle)



## T Latch cont.

T	Q <sup>+</sup>
0	Q
1	Q'

T	0	1
0	0	1
1	1	0

Problem  
T = 1  
Output Oscillates

Characteristic  
Equation

$$\begin{aligned} Q^+ &= TQ' + T'Q \\ &= T \oplus Q \end{aligned}$$