

Computer Science CSCI 355

Digital Logic and Computer Organization

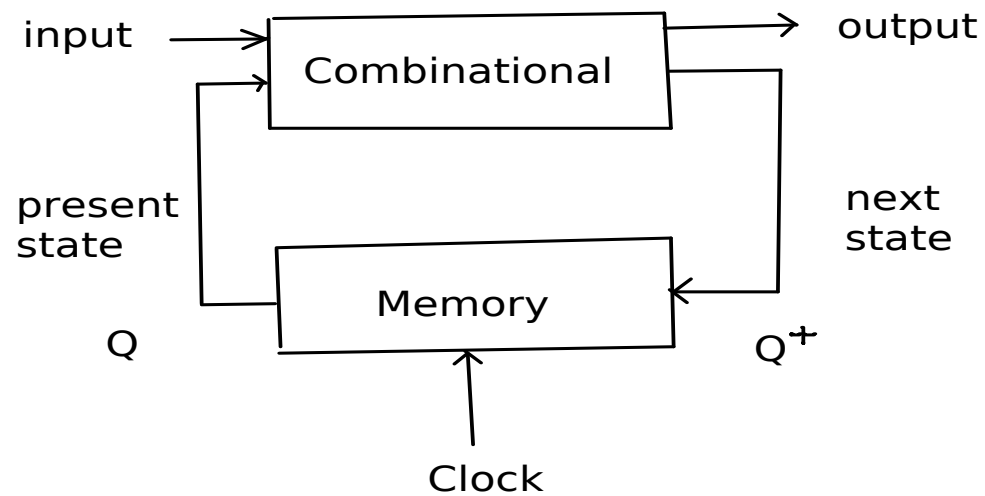
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Synchronous Sequential Design



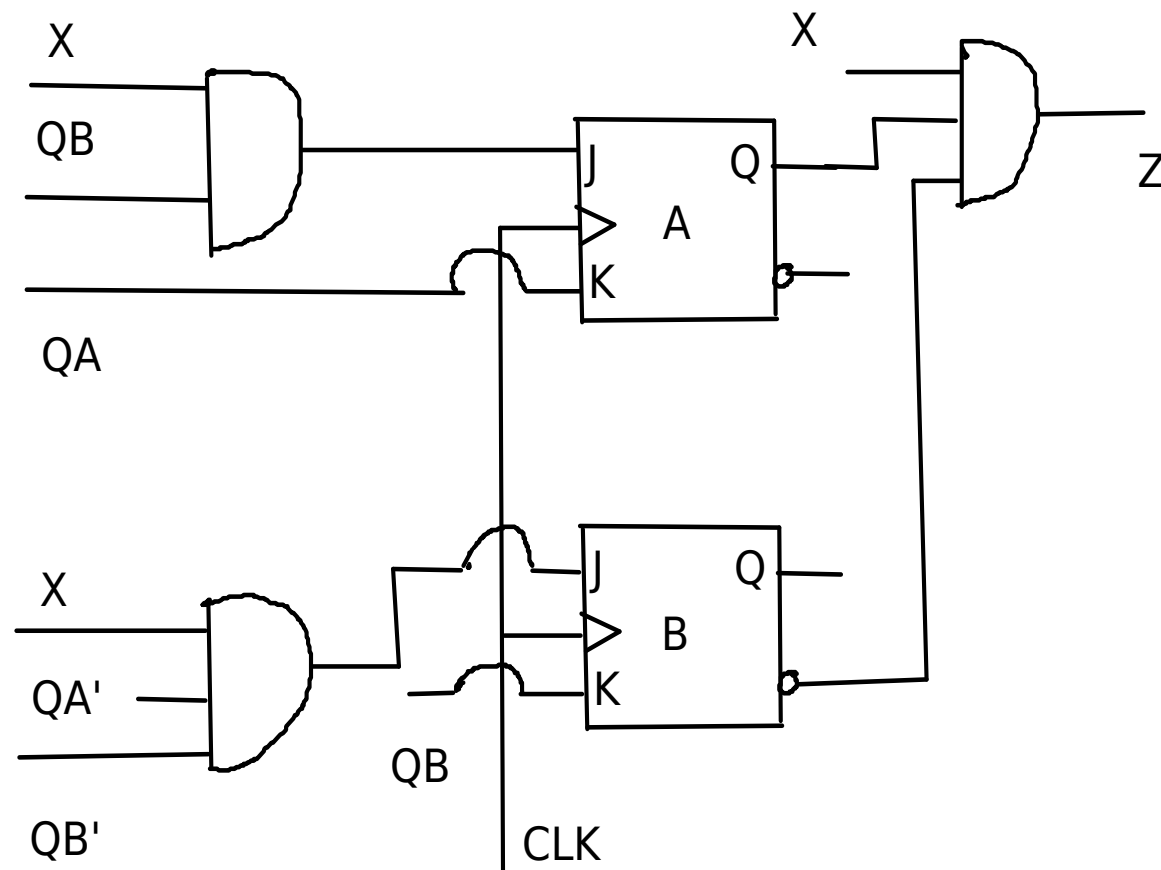
- Engineering Paradigm
 - Analyze
 - Design/Implement

FSM Symbolic Analysis

○ Algorithm

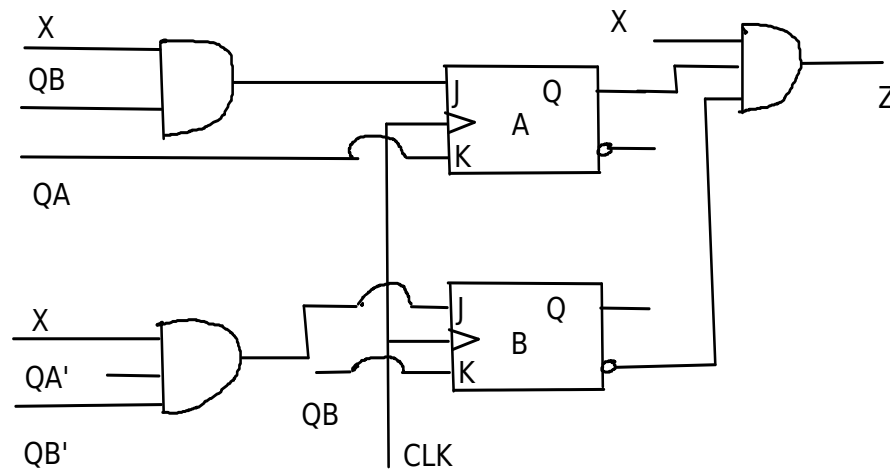
- 1. generate expressions describing outputs and FF inputs
- 2. generate next state equations for each FF
- 3. generate next state K maps for each FF and K maps for each output
- 4. generate a state table
- 5. generate state diagram or timing diagram

FSM Symbolic Analysis Example



Step 1

generate expressions describing outputs and FF inputs



$$\begin{aligned} Z &= X \cdot QA \cdot \overline{QB} & JA &= X \cdot QB \\ KA &= QA & JB &= X \cdot \overline{QA} \cdot \overline{QB} \\ KB &= QB \end{aligned}$$

Step 2a

generate next state equations for each FF

$$J_A = X Q_B \quad J_B = X \overline{Q_A} \overline{Q_B}$$
$$K_A = Q_A \quad K_B = Q_B$$

$$Q_A^+ = J_A \overline{Q_A} + \overline{K_A} Q_A$$

(Char. Eq.)

$$= X \cdot Q_B \cdot \overline{Q_A} + \overline{Q_A} \cdot Q_A$$

$$= X \cdot Q_B \cdot \overline{Q_A}$$

Step 2b

generate next state equations for each FF

$$J_A = X Q_B \quad J_B = X \overline{Q_A} \overline{Q_B}$$
$$K_A = Q_A \quad K_B = Q_B$$

$$Q_B^+ = J_B \overline{Q_B} + \overline{K_B} Q_B$$

(Char. Eq.)

$$= X \overline{Q_A} \overline{Q_B} \overline{Q_B} + \overline{Q_B} \cdot Q_B$$

$$= X \overline{Q_A} \overline{Q_B}$$

Step 3a

generate next state K maps for each FF and K maps for each output

$$QA^+ = X \cdot QB \cdot \overline{QA}$$

		QA QB			
		00	01	11	10
X	0				
	1		1		

(1,0,1)

Step 3b

generate next state K maps for each FF and K maps for each output

$$QB^+ = X \cdot \overline{QA} \cdot \overline{QB}$$

		QA QB			
		00	01	11	10
X	0				
	1	1			

QB^+

(1, 0, 0)

Step 3c

generate next state K maps for each FF and K maps for each output

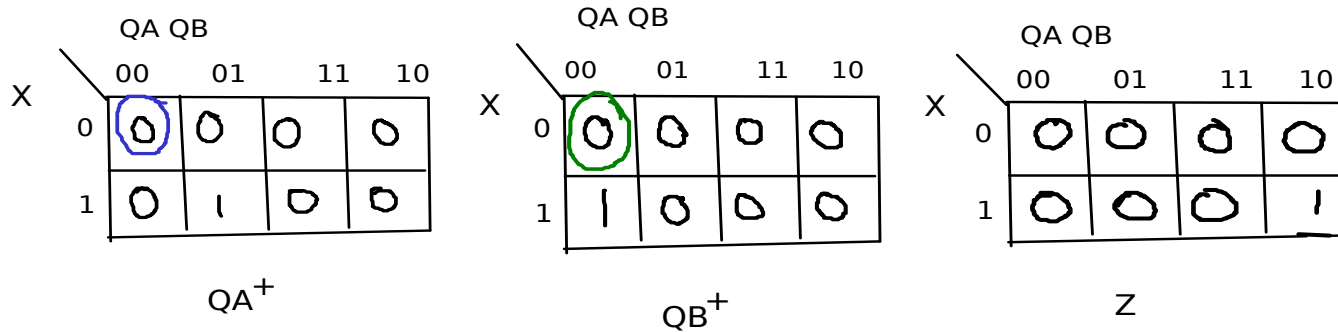
$$Z = X QA \overline{QB}$$

		QA QB			
		00	01	11	10
X	0				
	1				1

(1, 1, 0)

Step 4

generate a state table

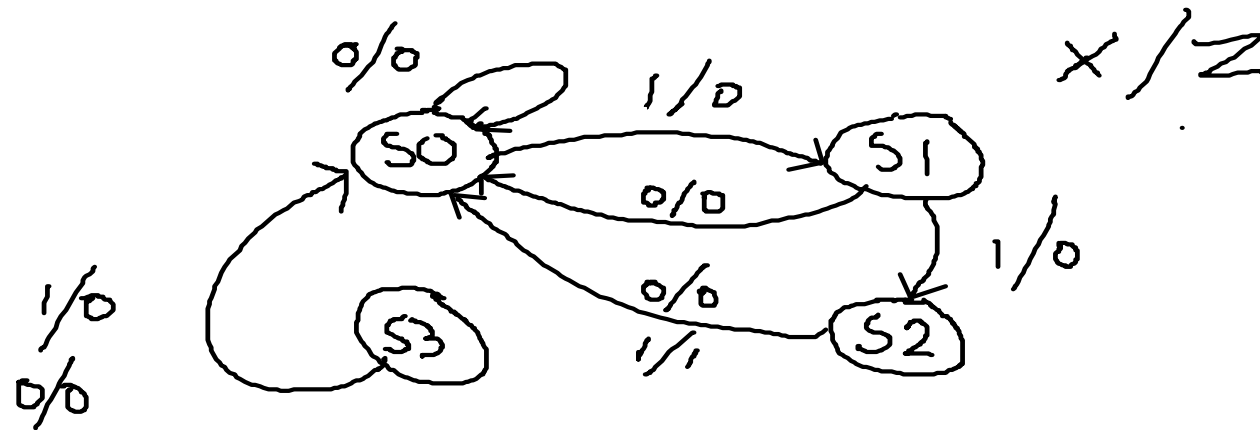


Present State		Next State		Output	
QA	QB	X=0	X=1	X=0	X=1
0	0	0	0	0	0
0	1	0	1	0	0
1	0	0	0	0	1
1	1	0	0	0	0

Step 5

generate state diagram or timing diagram

Present State			QA ⁺ QB ⁺ QA ⁺ QB ⁺		Next State		Output	
QA	QB		X=0	X=1	X=0	X=1	X=0	X=1
0	0	S0	00	01	0	0	0	0
0	1	S1	00	10	0	0	0	0
1	0	S2	00	00	0	1	0	1
1	1	S3	00	00	0	0	0	0



FSM Implementation

- Algorithm
 - r1. reverse the steps used in symbolic analysis up to (and including) step 3
 - r2. use excitation tables to determine FF inputs
 - r3. draw the resulting network diagram

Reverse Step 2a

use excitation tables to determine FF inputs

		QA QB			
		00	01	11	10
X	0	0	0	0	0
	1	0	1	0	0

QA⁺

Q	Q ⁺	J	K
0	0	0	-
0	1	1	-
1	0	-	1
1	1	-	0

		QA QB			
		00	01	11	10
X	0	0	0	←	—
	1	0	1	←	—

$$JA = XQB$$

		QA QB			
		00	01	11	10
X	0	—	←	↑	↑
	1	—	←	↑	↑

$$KA = QA$$

Reverse Step 2b

use excitation tables to determine FF inputs

		QA QB			
		00	01	11	10
X	0	0	0	0	0
	1	1	0	0	0

QB⁺

Excitation Table			
Q	Q ⁺	J	K
0	0	0	-
0	1	1	-
1	0	-	1
1	1	-	0

		QA QB			
		00	01	11	10
X	0	0	-	-	0
	1	1	-	0	0

		QA QB			
		00	01	11	10
X	0	-	1	1	-
	1	-	1	1	-

$$J_B = \overline{X} \cdot \overline{Q_A} \cdot \overline{Q_B}$$

$$K_B = Q_B$$