Computer Science CSCI 355

Digital Logic and Computer Organization

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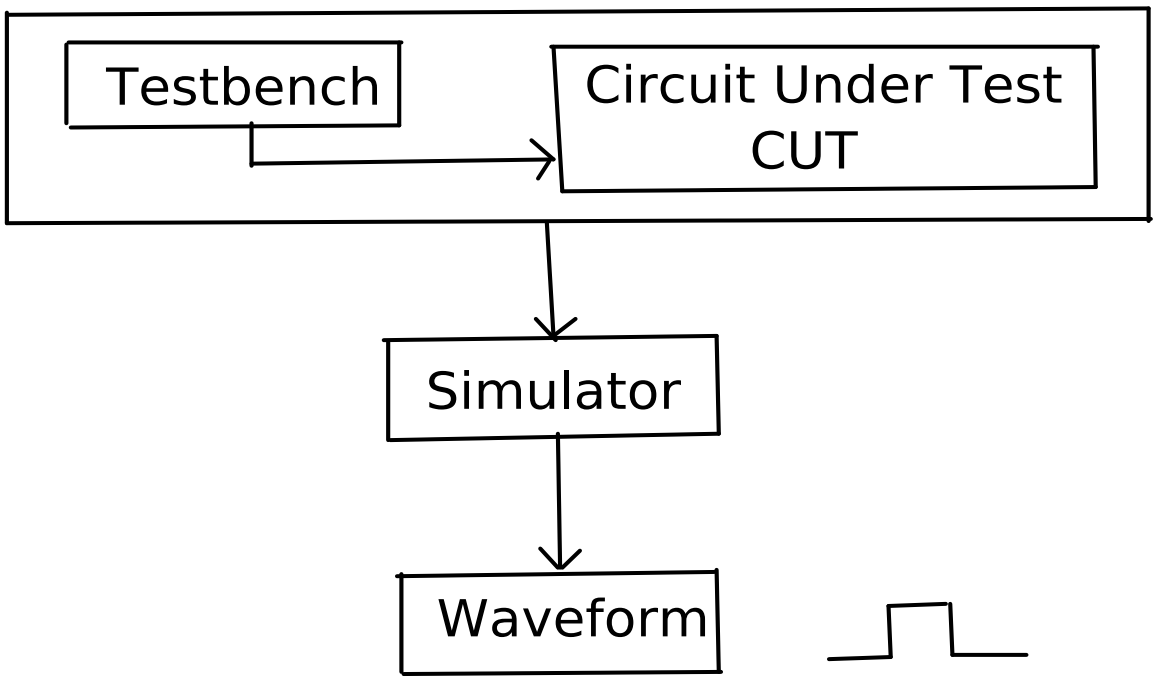
Hardware Description Languages (HDLs)

- Advantages
  - facilitate faster design
  - support design verification
  - used in simulation and synthesis
- Popular HDLs
  - Verilig (C like syntax)
  - VHDL (Pascal/Ada like syntax)
  - CSCI 355 will use Icarus Verilog

Verilog Simulation



Verilog Overview

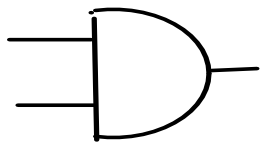
- Terminology
  - a *module* describes a hardware component
  - a *design* is described as a hierarchy of other modules
  - the top level module is the complete design (referred to as the CUT)
  - other modules are the design's components
  - components are interconnected using *ports*
  - systematic design testing is achieved using a *testbench*

Verilog Abstraction Levels

- Behavioural
  - system of concurrent components
  - describes behaviour only without regard to to implementation or structure
  - typically non-synthesisable
- Dataflow
  - characterized by register transfer or assignment
- Structural
  - component instantiation and inter-connection

Verilog Adder/Subtracter

- Logic Gate Review



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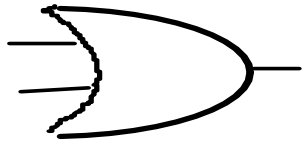

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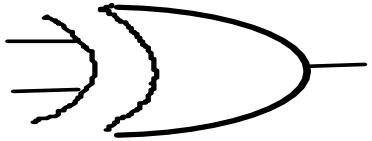


Xor

x	y	x.y
0	0	0
0	1	0
1	0	0
1	1	1

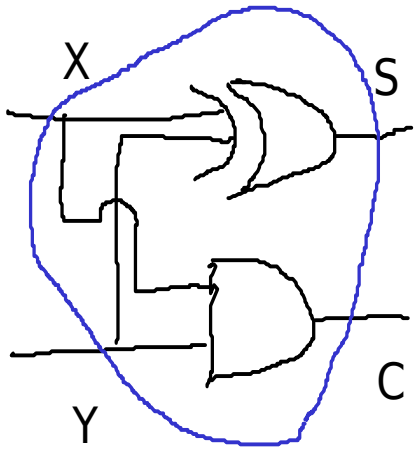
x	y	x+y
0	0	0
0	1	1
1	0	1
1	1	1

x	y	x xor y
0	0	0
0	1	1
1	0	1
1	1	0

Verilog Adder/Subtracter cont.

- Half Adder (HA)
  - combinational circuit to add two binary digits (bits)

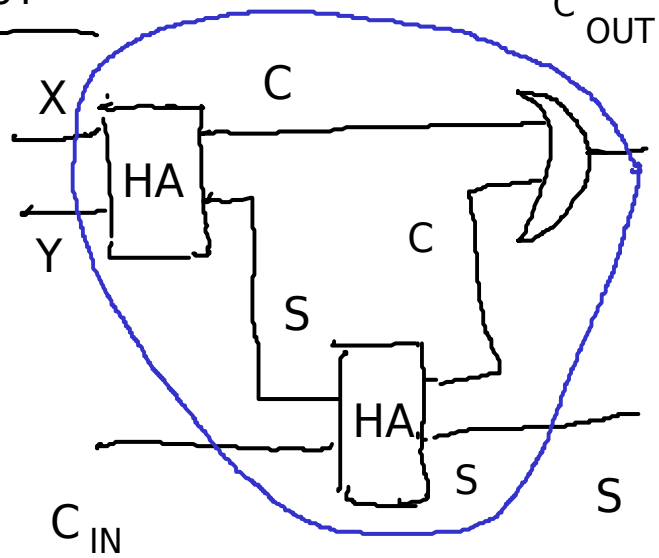
X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Verilog Adder/Subtracter cont.

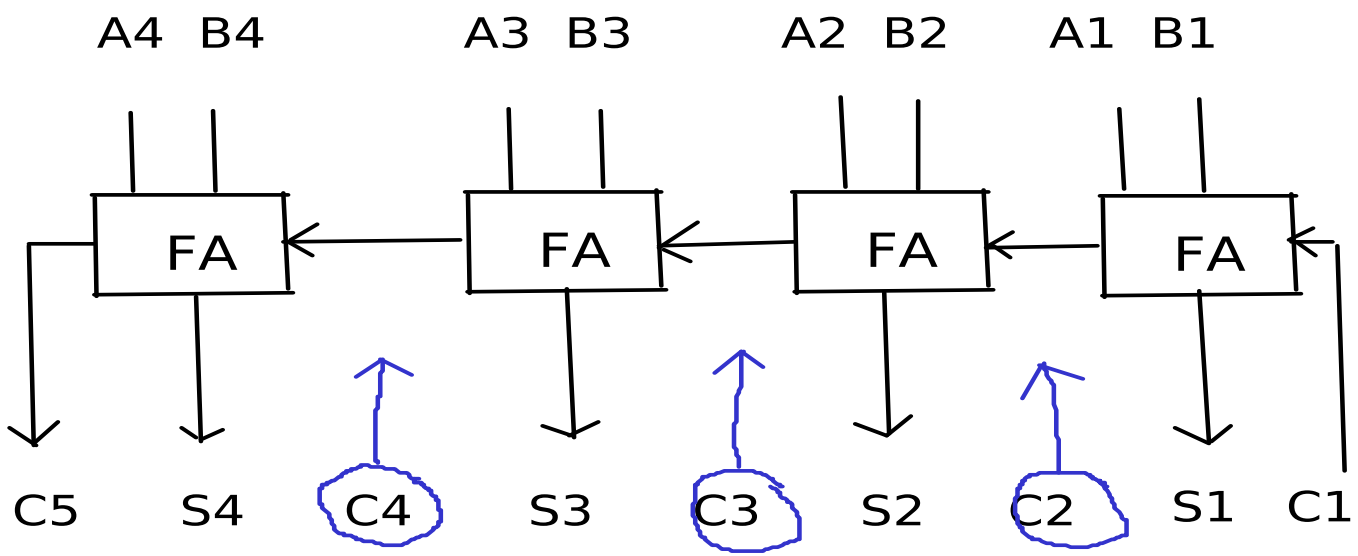
- Full Adder (FA)
  - combinational circuit to add three binary digits (bits)

X	Y	C_{IN}	S	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Verilog Adder/Subtracter cont.

- Ripple Cary Adder
  - combinational circuit to add 2 four bit numbers



Verilog Adder/Subtracter cont.

- Ripple Cary Adder/Subtracter
  - combinational circuit to add/sub 2 two bit numbers using 2's complement arithmetic