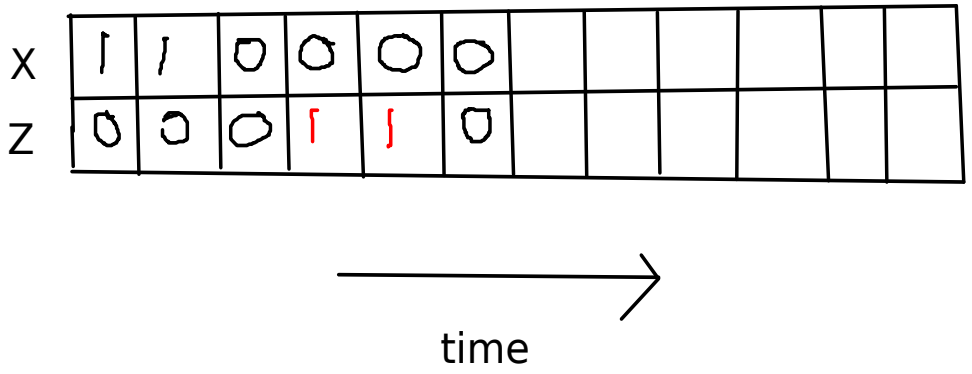
Computer Science CSCI 355

Digital Logic and Computer Organization

Dr. Peter Walsh
Department of Computer Science
Vancouver Island University
peter.walsh@viu.ca

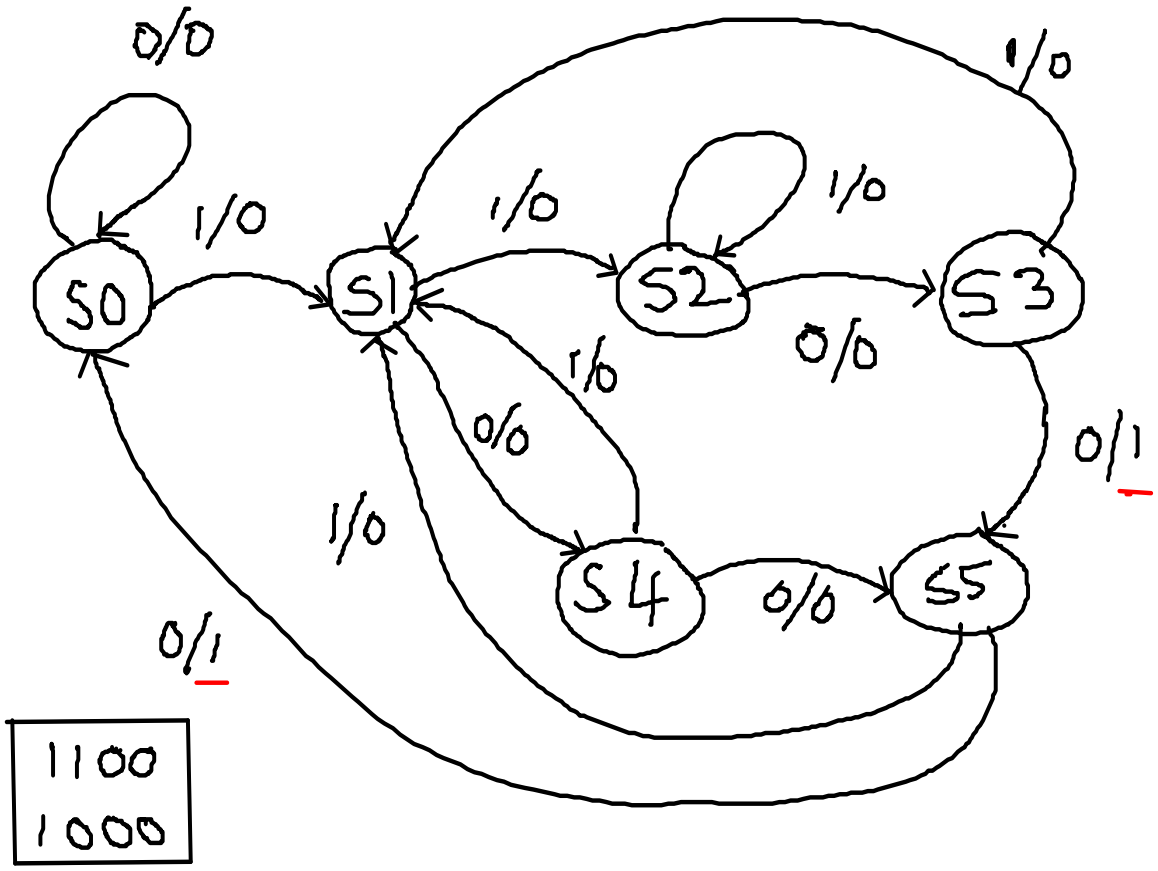
Non Resetting Sequence Detector

Task: design and construct a non-resetting sequence detector to detect the sequences 1100 or 1000 using D edge triggered flip flops.

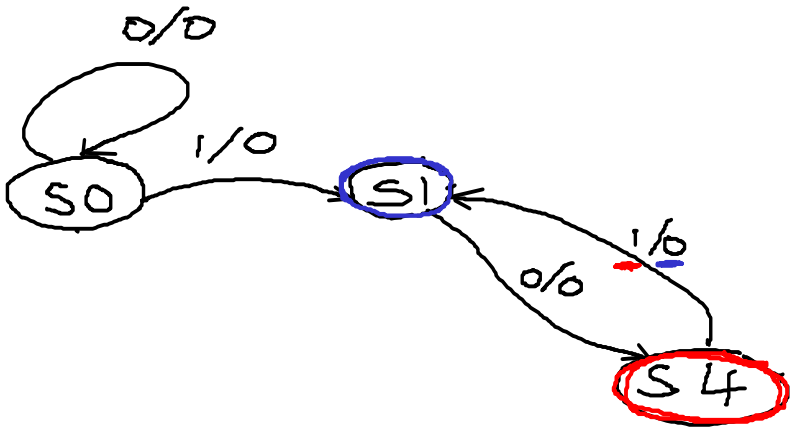


One input X. One output Z.

FSM (Step 5)



State Table Construction (Step 4)



Present State	Next State		Output		Encoding		
Q	Q+		Z		QA	QB	QC
	X=0	X=1	X=0	X=1			
S0	S0	S1	0	0	0	0	1
S1	S4		0		1	0	1
S4		S1		0			

State Table (Step 4)

Present State	Next State		Output		Encoding		
Q	Q+		Z		QA	QB	QC
	X=0	X=1	X=0	X=1			
S0	S0	S1	0	0	0	0	1
S1	S4	S2	0	0	1	0	1
S2	S3	S2	0	0	1	1	1
S3	S5	S1	1	0	0	1	0
S4	S5	S1	0	0	0	1	1
S5	S0	S1	1	0	0	0	0

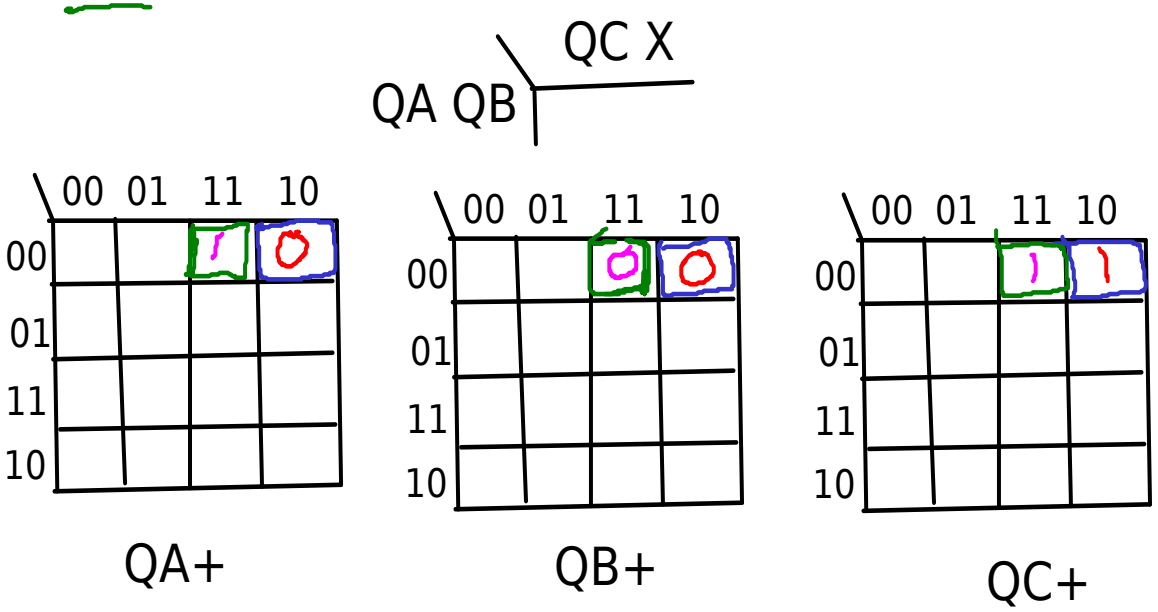
State Table cont. (Step 4)

QA QB QC

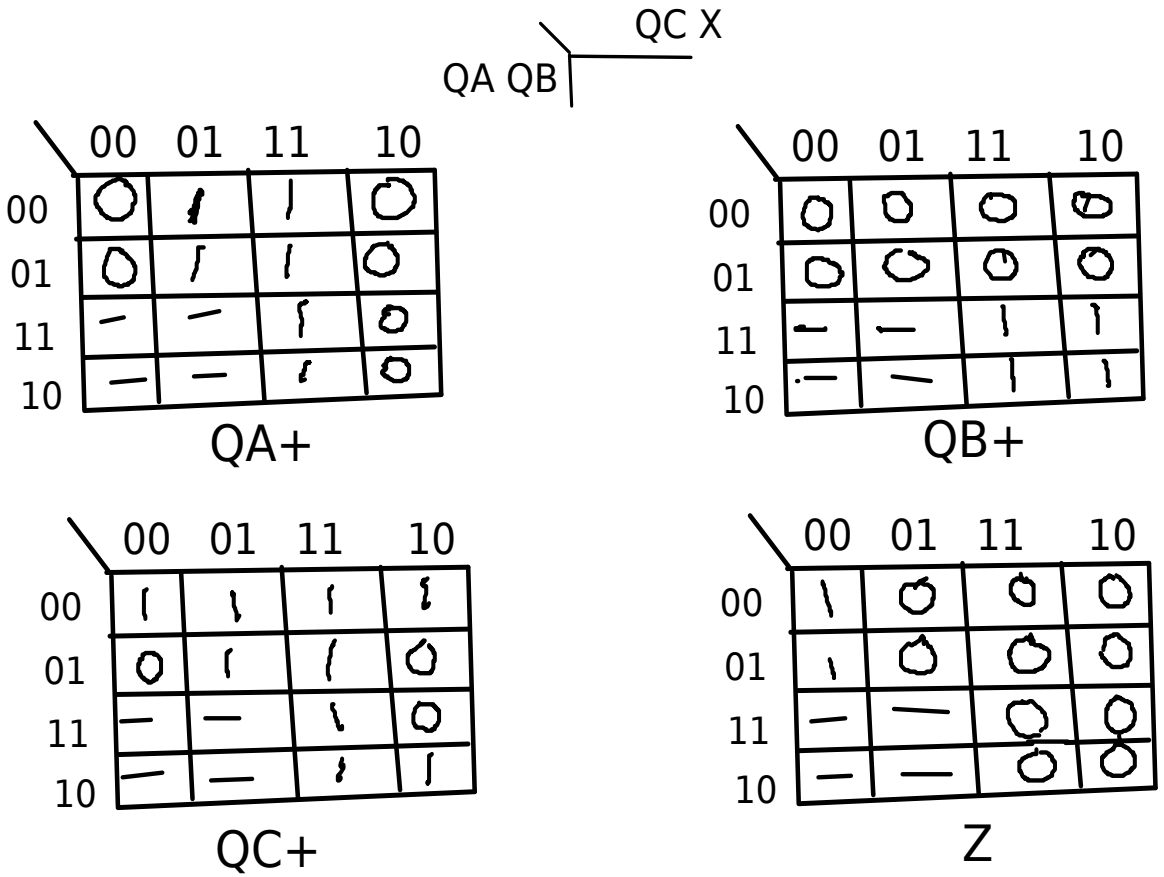
Present State Q		Next State Q+		Output Z	
		X=0	X=1	X=0	X=1
001	S0	001	101	0	0
101	S1	011	111	0	0
111	S2	010	111	0	0
010	S3	000	101	1	0
011	S4	000	101	0	0
000	S5	001	101	1	0

K Map Construction (Step 3)

Q	Q+		Z	
QA QB QC	X=0	X=1	X=0	X=1
001	001	101	0	0



K Map Construction (Step 3)

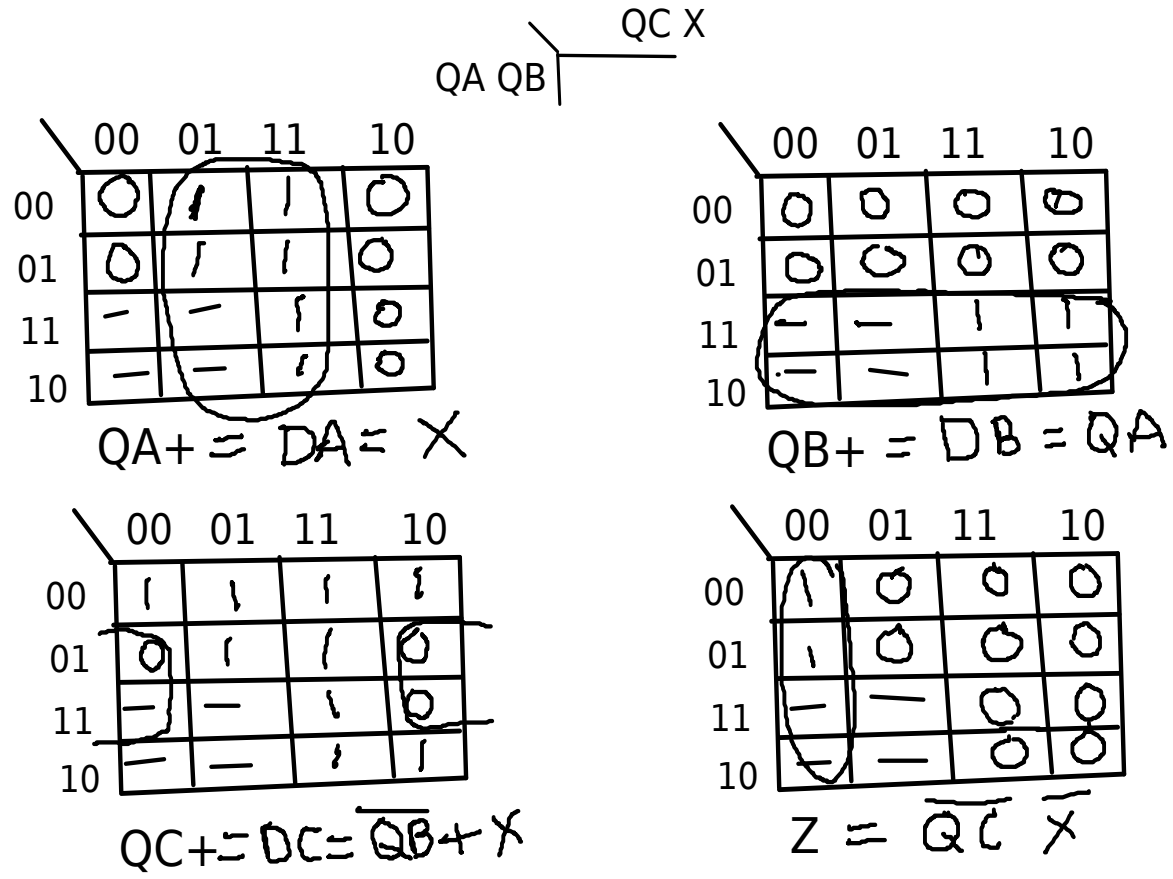


Excitation Tables)

Q	Q+	S	R	J	K	T	D
0	0	0	-	0	-	0	0
0	1	1	0	1	-	1	1
1	0	0	1	-	1	1	0
1	1	-	0	-	0	0	1

$Q^+ = D$

FF-Input And Output Eq. (Step 2)



Circuit Diagram (Step 1)