

VANCOUVER ISLAND UNIVERSITY
FINAL EXAMINATION DECEMBER 2015
COMPUTING SCIENCE CSCI 355

Instructor: Dr. P Walsh **Duration:** 3 Hours.

TOTAL VALUE	100				
QUESTION	1	2	3	4	5
VALUE	5	25	25	25	20

Instructions

- Students must count the number of pages in this examination paper before beginning to write, and report any discrepancy immediately to the invigilator.
- This examination paper consists of 3 numbered pages not including this cover page and additional pages relating to the SSBC (SSBC's Data Flow Diagram, Abstract RTN and Control Signal list).
- Answer all questions in an answer booklet. All questions relate to material covered in class or in the lab. Show all your work.
- This is a CLOSED BOOK - examination. Students may consult notes written on one 8in. by 11 in. sheet of paper as described in class.
- Calculators are NOT permitted.

QUESTION 1.

Let

$$F(A, B, C, D, E) = \Sigma m(0, 2, 3, 4, 8, 10, 11, 12, 16, 18, 19, 20, 24, 26, 27, 28)$$

- (a) Find the minimal SOP expression for F.
- (b) Find the minimal POS expression for F.

QUESTION 2.

Consider the situation where a synchronous FSM implementation has one input (x), one output (z) and two D edge-triggered flip flops (A and B).

- (a) Derive the state-transition and output table for the machine given that

$$D_A = \bar{x} Q_B$$

$$D_B = x \overline{Q_A} \overline{Q_B}$$

$$z = \bar{x} Q_B$$

- (b) Reimplement the FSM using edge-triggered SR flipflops.

QUESTION 3.

Consider the following state-transition table.

Present State	Next State			
	$XY=00$	$XY=01$	$XY=10$	$XY=11$
a	b	b	b	b
b	c	e	g	g
c	d	d	d	d
d	e	e	d	d
e	f	f	f	f
f	a	a	g	g
g	g	g	e	b

Your task is to implement the state transitions using the counter specified below and some glue logic.

To this end, you must derive minimized input equations for the counter inputs.

Note 1: You must use the following state assignment table.

State	Encoding
a	000
b	001
c	010
d	011
e	100
f	101
g	110

Note 2: Counter operations have a priority with "load" having the lowest priority. If you have a choice of operation to achieve a particular next-state then you must choose the operation with highest priority.

In addition to the counter, you may use other logic gates as necessary (all equations should be minimized).

```
module counter(LOAD, CE, SCLR, CLK, L, Q);
```

```
    input LOAD, CE, SCLR, CLK;
    input [2:0] L;
    Q [2:0] count;
```

```
    ...
```

```
endmodule
```

LOAD	CE	SCLR	L[2:0]	Operation	Priority
1	0	0	load value	load	0
0	1	0	xxx	count up	1
0	0	1	xxx	clear	2
0	0	0	xxx	no-operation	3

Note 3: 'x' means dont-care.

QUESTION 4.

Consider the state-transition table from the previous question. Your task is to implement the state transitions using three edge triggered D flip flops, three 8-to-1 data selectors (multiplexors) and some glue logic.

To this end, you must derive minimized input equations for the data selector inputs and flip flop inputs.

Note: Let the current state variables be labelled Q_A , Q_B and Q_C . You are required to place these variables, in order, on the control lines of the multiplexors where Q_C is the least significant select bit.

QUESTION 5.

(a) Consider the following state-transition and output table. It has one input X and two outputs Y and Z . Your task is to identify any equivalent states.

Present State	Next State		Output Y Z
	$X=0$	$X=1$	
a	a	b	1 0
b	a	b	0 1
c	d	f	0 0
d	a	h	1 0
e	f	d	0 0
f	c	b	1 0
g	a	b	0 0
h	d	b	0 1

(b) With regard to the Stack Machine (SSBC), consider SSBC's Data Flow Diagram, Abstract RTN and Control Signal list. You are to assume that the SSBC's control unit (CU) and memory sub-system are sensitive to the rising edge of the clock. In addition, you may assume a read/write cycle will complete in one CU clock cycle.

Develop a complete FSM to implement the *nor* instruction (instruction fetch and execution).