Experiment 10

The SSBC (Stack Single Board Computer) is an 8 bit machine with a 16 bit address space used to explore computer architecture concepts in csci 261 and computer organization concepts in csci 355. Its design, behavioural implementation and verification are detailed in the work-products:

- Abstract RTN
- Data Flow Diagram
- Perl Simulator
- Perl Simulator test plan and test implementation
- Perl Simulator example programs
- Verilog Behavioural Model (control unit, data path and memory)
- Control Signals
- Verilog test plan and test implementation
- Verilog Behavioural Model example programs

The MMA (Modified Manchester Architecture) is a 16 bit machine with a 12 bit address space. Starting with an ARTN specification (`Lab10/Doc/mma-v1-r2.artn`), your task is to develop a similar set of work-products to the ones listed above for the MMA. You are free to add registers to the architecture as you see fit.