Experiment 5

Develop a 4 bit adder/subtractor by augmenting a 4 bit binary adder and then, augmenting the adder/subtractor to yield a 4 bit magnitude comparator. The comparator has two 4-bit inputs (`A` = `A1` through `A4` with `A1` the MSB and `B` = `B1` through `B4` with `B1` the MSB) and and three 1-bit outputs `x, y, z`. The comparator outputs are derived from the outputs of the subtraction `A - B` as follows. If `(A-B)` is equal to zero then `A=B`; assert `x` and deassert `y` and `z`. If `(A-B)` yields no carry-out (borrow) then `A<B`; assert `y` and deassert `x` and `z`. If `(A-B)` is not equal to zero and the subtraction yields a carry-out (borrow) then `A>B`; assert `z` and deassert `x` and `y`. Note, the comparator outputs are active high.

Task: Design a 4-bit comparator.

Deliverable (D1): Annotated logic schematic for the comparator. Note, use adder's logic symbol in your schematic.

Task: Develop a structural Verilog model of the comparator using the Verilog models for the TTL ICs SN7486, SN7404, SN7408 and SN7483.

Deliverable (D2): Electronic submission of source code (`make submit`).

Task: Map your Verilog model to a TTL-based physical design for the combinational system.

Deliverable (D3): IC logic schematic.

Task: Specify IC interconnections.

Deliverable (D4): One completed pin-out sheet (at least) for each IC employed in your physical design.

Task: In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D5): A physical realization of the combinational system that behaves to specifi-

cation. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task: Document any relevant results, explanations or comments.

Deliverable (D6): A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

NOTES